Master Thesis & Internship Projects @ imec

2016 - 2017 Topic Guide

Information

Students from universities and engineering schools can apply for a Master thesis and/or internship project at imec. Imec offers topics in engineering and (industrial) sciences in different fields of research.

All Master internship and thesis projects currently available at imec are collected in this topic guide. The projects are classified according to the imec research domains. You can find more detailed information on each research domain under the heading 'R&D Offering' on www.imec.be.

How to apply?

Send an application e-mail including your motivation letter and detailed resume to the responsible scientist(s) mentioned at the bottom of the topic description you choose.
The scientist(s) will screen your application and let you know whether or not you are selected for a project at imec. It is not recommended to apply for more than three topics.

There is no application deadline. We accept applications at any time and deal with them throughout the year.

Master internship students usually receive an allowance. However, some research groups only accept self-supporting students. Do you want to know upfront whether the project you wish to apply for provides financial support? When sending in your application email check the remuneration details with the responsible scientist.

For more information, go to the Master thesis & internship section on the Work at imec tab on www.imec.be. Do you have additional questions, then send an email to student@imec.be.

For Master thesis/internship projects in **imec the Netherlands** refer to
http://www.holstcentre.com/careers/thesis-opportunities or contact talent@imec-nl.nl.

After acceptance

In case of acceptance to our internship program you are sure to embark on a very exciting and interesting experience! For imec, your contribution as a student will be essential in meeting the deliverables in our programs. Therefore, it is vital that - once you accept to come to imec - we can count on your commitment and dedication for the entire duration of the internship period.

I. CMOS Scaling

3D interconnect-based segmented bus architecture modelling and exploration

The communication and memory organisation in internet gateways and servers are a major source of energy consumption. Future technologies will lead to higher performances but also to an increased energy bottleneck. In this thesis, we want to build an exploration framework for comparing different 3D interconnect-based options for emerging processor and memory communication architectures. The main goal will be to reduce the overall energy consumption for given application workloads executed on this communication and memory architecture. Simulations will be performed based on available measurement data to calibrate the energy and performance models.

Profile: Strong interest in architecture exploration and simulation, basics of microelectronic technologies with emphasis on 3D interconnect schemes

Type of project: Internship project of 6 months (full-time, at imec Leuven)
The start date of the project is Q2/Q3, 2017

Degree: Master in Engineering majoring in computer architecture or micro-electronics

Responsible scientist(s):
For further information or for application, please contact Eric Beyne (Eric.Beyne@imec.be) and Francky Catthoor (Francky.Catthoor@imec.be).

Study of the kinetics of chemical reactions in nanostructures

In semiconductor manufacturing, new generations of devices have entered the nano-world, with critical dimensions smaller than 100 nm. Many process steps are still performed using aqueous chemistries, e.g. wet etching of materials for patterning and wet cleaning of surfaces. New transistor geometries are vertical, with the generation of 1-D and 2-D nano-confined spaces (Fig. 1). Little is known about the kinetics of chemical reactions in nano-confined volumes. Chen et al. (2009) showed that the rate of enzymatic reactions was increased in nano-vesicles, while Okuyama et al. (2015) obtained a decreased etching rate for 1-D confined SiO2 nano-layers. Mechanisms affecting reaction kinetics at the nano-scale are not well understood. Chen et al. (2009) suggested that both an increased enzyme-substrate collision frequency and the enzyme-vesicle wall interactions may affect the reaction rate, while Okuyama et al. (2015) proposed that surface charges affected the concentration of reactive ions in the nano-slit.
In this project we investigate the kinetics of chemical reactions in nano-holes with 2-D confinement (Fig. 2). In a first part the etching behavior of metallic layers covering the wall of nano-holes with varying diameter will be studied (e.g. TiN using ammonia-hydrogen peroxide mixtures). The student will perform the wet etching tests, the data treatment of TEM (transmission electron microscopy) pictures generated by operators in the pilot-line, and a kinetic analysis. Results will be compared to etch rates obtained on planar films with film thickness measured by ellipsometry. In a second part the kinetics of reactions involving a SAM (self-assembled monolayer) deposited on the structures will be studied using ATR-FTIR (attenuated total reflection Fourier-transform IR spectroscopy). The method has already been developed and tested on nano-lines with 1-D confinement, where a rate increase of 30% was observed. Here the student will prepare the ATR crystals (polishing), perform the FTIR tests using a home-build liquid cell, as well as the data treatment and interpretation. The content of the student project will be adapted depending on the progress of our research.

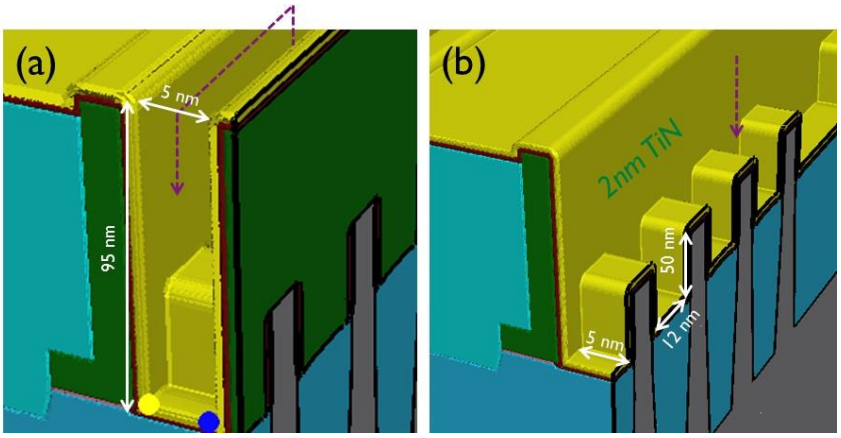


Figure 1. Cross-sections in a cartoon of a FINFET transistor after removal of the dummy gate (not to scale), showing (a) a nano-slit with 1-D confinement, (b) nano-holes with 2-D confinement.

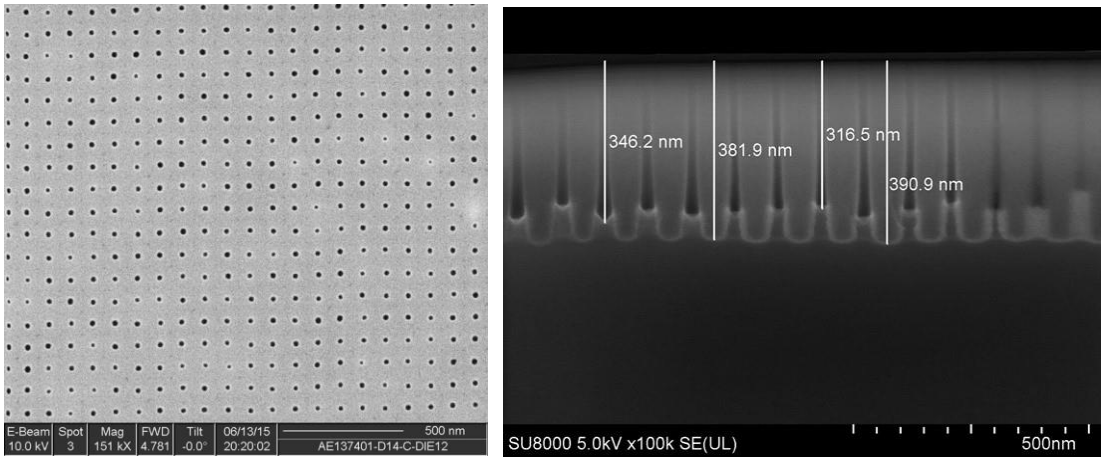


Figure 2. SEM images of nanoholes: (left) top view, (right) cross-section view.

Type of project: Thesis or internship project or combination of both

Degree: Master in Industrial Sciences and Master in Science and Master in Engineering majoring in chemistry/chemical engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Guy Vereecke (guy.vereecke@imec.be).

3D chemical analysis of microelectronics systems

One driver of the semiconductor industry growth is the sustained realization of "Moore's Law", whereby the number of transistors in an integrated circuit doubles approximately every 2 years with an associated increase in circuit functionality, reduction in operational power, and, most important, a reduction in unit cost. These fast technological developments, including increased process and material complexity, as well as reduced tolerance levels for process excursions have increased the need for a more controlled manufacturing environment necessitating equivalent improvements and developments in metrology. The present evolution towards merging lab and Fab metrology implies that these developments are necessary for use both in the R&D phase as in the final production phase.

With the strong size dependence of many material problems and phenomena, metrology needs to be performed more and more on devices with realistic dimensions and on wafer scale.
Imec has recently acquired a new metrology tool combining a TOF-SIMS (Time of Flight Secondary Ions Mass spectrometry) and an AFM (Atomic Force Microscope) instrument. This instrument is designed in order to combine chemical information from the TOF-SIMS with topographical information from the AFM, allowing 3D chemical mapping of samples.
The objective of this thesis is to establish this AFM/TOFSIMS system as a 3D-metrology tool. For this objective, the AFM module will be used purely in topographic mode.
The first part of the thesis will be devoted to the qualification of this new instrument to establish its ultimate performances, before applying it to model system. These systems will be chosen from technologies from the Back-End-OF-Line (dual damascene). In these systems, etching of trenches occurs via a Reactive Ion Etching step, leaving polymer residues on the structures. These residues need first to be cleaned before metal deposition can occur and a detailed chemical analysis is frequently needed to determine the optimum cleaning process and its efficiency. This can be evaluated by XPS on specifically designed structures . However, the information content of TOFSIMS for organic contaminants is much higher than from photoemission, hence TOFSIMS is a preferred analysis approach. Unfortunately, the topography on the line arrays prevents a full 3D reconstruction of TOFSIMS profiles. The application of the 3D-TOFSIMS system using the in-situ AFM represents an important step forward in this case. After filling the trenches with Cu, one still has no or limited physico-chemical information on the 3D Cu concentration in the ILD between Cu lines. A prominent challenge one faces in analyzing these structures, is that when using sputtering for depth profiling, topography is developing during the analysis due to large difference in erosion rate between the different materials. This thesis will show that this problem can be solved using TOFSIMS-AFM by monitoring the topography growth and implementing correction procedures. The output will be protocols for quantitative composition profiles for heterogeneous and non-planar systems.

Type of project: Thesis with internship project

Degree: Master in Science and Master in Engineering majoring in chemistry/chemical engineering, physics, materials engineering

Responsible scientist(s):
For further information or for application, please contact Thierry Conard (tconard@imec.be), Wilfried Vandervorst (vdvorst@imec.be) and Alexis Francquet (Alexis.franquet@imec.be).

Seeding and growth of boron-doped diamond thin films

Diamond is outforming other materials in many domains such as hardness, wear resistance, thermal conductivity, chemical inertness, and biocompatibility. As it can be made electrically conductive (p-type) by boron doping, boron-doped diamond thin films look especially attractive for electrical applications. They are being explored and developed for a wide range of applications including chemical treatment (e.g. waste water, swimming pool, chemical solutions), nanoscale electrical probes, implantable bio-electrodes, and water splitting/hydrogen generation.
The goal of this internship is to obtain better insight into the interfacial growth of boron-doped diamond layers. For this, the student will seed and grow diamond layers using imec's hot-filament chemical vapor deposition (HFCVD) reactor using different doping levels, seeding densities and growth parameters. The electrical analysis at the nanoscale is carried out on the interfacial side using electrical AFM methods such as SSRM and conductive AFM (c-AFM) for studying the grain and grain-boundary conductivity. Here, we look for a correlation between boron doping level and grain conductivity. Furthermore, a comparison of doped versus undoped diamond seed nano-crystals is done. The conversion of a seed layer into a highly conductive interfacial layer is not completely understood yet and is therefore investigated in detail in this study. For physical analysis, scanning electron microscopy (SEM), RAMAN, and elastic recoil detection (ERD) are used.
For this topic, the student will work inside a lab and cleanroom environment to carry out the required experimental steps. He/she will characterize the fabricated samples by different characterization techniques. The student will be part of imec's materials and component and analysis group.

Type of project: Thesis or internship project or combination of both

Degree: Master in Science and Master in Engineering majoring in chemistry/chemical engineering, physics, materials engineering, electrotechnics/electrical engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Thomas Hantschel (thomas.hantschel@imec.be).

Parallel processing application for iba data analysis

Imec does research on a wide variety of front edge micro-electronic devices and applications (transistors, memories, solar cells,...). To verify the correct fabrication of these extremely challenging new devices (sub-22 nm technology) also high end characterization tools are essential. In this framework accelerator based characterization is one of the approaches that is pursued. For this, imec operates a 2 million Volt tandem particle accelerator, connected to multiple beam-lines and detection end-stations (vacuum chambers) maintained at high vacuum. The experimental results (spectra) are compared to physical models to quantify the properties of the fabricated devices.
As of now, the optimization of the model towards the experimental result is achieved by least squares fitting (fitting) using the grid-search or Levenberg-Marquardt algorithm. This has been realized by researchers at imec. Due to the computational demand, only a few parameters can be fitted (at once), and the analyst needs to supervise and steer the analysis constantly – a lengthy and labor intensive activity.
The purpose is develop a new software program for the analysis of the experimental results. The student will implement new algorithms for the optimization that lend themselves better towards parallelization, for example the differential evolution algorithm. Besides, the student will also prepare the necessary code to allow for parallel operation on multiple cores and demonstrate its advantages.
The main tasks will be:

- To implement alternative optimization algorithms, for example the differential evolution algorithm.
- To investigate the performance of the new optimization method.
- To prepare the new program to allow its execution on multiple cores.

This subject is an opportunity for those who wish to get in-depth experience on the aspects of multi-core and parallel processing, on data analysis and on computational optimization.

Type of project: Thesis or thesis with internship project

Degree: Master in Industrial Sciences and Master in Science and Master in Engineering majoring in physics, electrotechnics/electrical engineering, nanoscience & nanotechnology, computer science

Responsible scientist(s):
For further information or for application, please contact Johan Meersschaut (johan.meersschaut@imec.be).

Embedded distributed human-machine application for accelerator based metrology

Imec does research on a wide variety of front edge micro-electronic devices and applications (transistors, memories, solar cells,...). To verify the correct fabrication of these extremely challenging new devices (sub-22 nm technology) also high end characterization tools are essential. In this framework accelerator based characterization is one of the approaches that is pursued. For this, imec operates a 2 million Volt tandem particle accelerator, connected to multiple beam-lines and detection end-stations (vacuum chambers) maintained at high vacuum.
This subject involves the implementation of a distributed embedded control application to enable the accelerator based metrology at imec. This project aims at the development of a new software package for the control of the system in a modular and naturally multi-threaded concept. In particular, the software allows to communicate with

single devices through Ethernet (TCP/IP) and RS232/RS485 (via Serial-Ethernet gateways) and with the user through a user-friendly graphical interface (GUI) as well as support for a flexible scripting language capability.
The software architecture is designed such that new devices can be connected and disconnected dynamically during the operation, and the devices appear as virtual instruments on the screen. The signals from various virtual instruments are accessible to both the GUI as well as to scripts that can be run in a command-like environment.
The main tasks will be:

- To implement communication drivers, so-called daemons, (with stepper motors, data acquisition, counters) in the Visual C++ environment using WinForms.
- To implement a graphical user interface in HTML + Javascript to run with Windows' Hypertext Application environment (HTA)
- To implement the same functionalities in Javascript to run in the console with node.js

Optionally, the student may investigate and introduce the novel concept of in-line analysis in ion-beam metrology. With this, we mean that an automatic data-treatment is initiated whenever new experimental results are obtained. The algorithms to perform the analysis are available at imec, but at this moment the analysis has to be initiated manually by the analyst.
This subject is an opportunity for those who wish to experience the aspects of programming within a Visual C++, Javascript, HTA, and node.js based environment for the development of human-machine interfacing and automation.

Type of project: Thesis or thesis with internship project

Degree: Master in Industrial Sciences and Master in Science and Master in Engineering majoring in physics, electrotechnics/electrical engineering, nanoscience & nanotechnology, computer science

Responsible scientist(s):
For further information or for application, please contact Johan Meersschaut (johan.meersschaut@imec.be).

One-dimensional carrier profiling of blanket and confined semiconducting structures

The performance increase of Complementary Metal Oxide Semiconductor (CMOS) devices at every new technology node has required to shrink their dimensions to the nanoscale and to introduce new high-mobility channel materials (Ge, SiGe, III-V). More recently, these devices have also moved from planar to three-dimensional architectures. In this context, it is urgent to develop a characterization technique able to accurately determine the incorporation and activation of dopants in the ultra-shallow doped regions of the transistors, i.e. the source, drain and extensions. This project aims at tackling this critical issue by combining two established techniques, i.e. Secondary Ion Mass Spectrometry (SIMS) and microhall (MH).
SIMS is the established technique for one-dimensional dopant profiling. In a nutshell, SIMS is based on the layer-by-layer sputtering of the sample with the help of a low-energy ion beam. The fraction of the sputtered atoms which are ionized is accelerated by an electric field to a mass spectrometer, where each species is separated and counted. Unfortunately, SIMS does not capture any electrical information about the sample as it measures the total dopant profile, i.e. including the inactive portion. In this project, we propose to incorporate multiple MH measurements during the sample sputtering to determine the active doping concentration at different stages of the profiling.
This project will essentially consist of two tasks. Task I will deal with simple blanket structures of doped Si and more advanced SiGe, Ge and III-V materials. MH measurements will be run either on the sputtered surfaces or on dedicated metallic pads to improve the electrical contacts. Task II will extend the technique to confined three-dimensional volumes. For this purpose, dedicated structures have been fabricated, where fin arrays of dimensions compatible with SIMS have been electrically connected in parallel such that their electrical resistance can be measured. In both tasks, the candidate will focus on the MH measurements and simulations. Calculations will indeed also be needed to understand the impact of the contact geometry and of the confinement on the free carriers and currents inside the investigated structures.
This work will be done in the characterization group of imec disposing of a multitude of characterization techniques in support of this project. It will also be done in very close collaboration with the process engineers of imec and its industrial partners.

Type of project: Thesis or internship project or combination of both

Degree: Master in Science and Master in Engineering majoring in physics, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Janus Bogdanowicz (janusz.bogdanowicz@imec.be).

Diamond probes for nanoscale electrical measurements

Diamonds superior properties in terms of hardness, thermal conductivity and chemical inertness make it an excellent engineering material for many applications. It can be made electrically conductive by boron doping. Over the last decade, boron-doped diamond tips have become the ultimate choice for performing electrical measurements on the nanometer scale with high spatial resolution. In contrast to other diamond applications where it faces a strong competition from other materials, doped diamond is really the only material which is able to withstand the extremely high pressures (in the GPa range) needed to establish a good electrical contact on silicon and germanium. The solid diamond tips are made by so-called molding whereby first a pyramidal pit is etched, then it is filled up with diamond and finally the mold is etched away. The pyramidal tip is attached to the end of a metal cantilever beam. Using such probes, state-of-the-art semiconductor device structures can be electrically characterized with nanometer spatial resolution.
The aim of this internship is the development of diamond tips probes with improved spatial resolution and electrical conductivity compared to the existing probes. The probes will be designed, fabricated and evaluated. For this topic, the student will work inside a cleanroom environment to carry out the required microfabrication steps. He/she will characterize the prototype probes by different characterization techniques. The student will be part of imec's materials and component and analysis group.

Type of project: Thesis or internship project or combination of both

Degree: Master in Science and Master in Engineering majoring in physics, chemistry, electrotechnics/electrical engineering, materials engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Thomas Hantschel (thomas.hantschel@imec.be).

Strain characterization inside advanced nano-electronics device structures by nano-focused Raman spectroscopy

Strain engineering is used as a concept in most advanced nanoelectronics transistor structures to enhance the mobility of electrons (or holes) in the channel region and thereby increasing the channel conductivity. This is achieved by various approaches (e.g. strain-inducing capping layers, using a silicon-rich solid solution such as SiGe). PMOS and NMOS respond differently to the applied strain. PMOS benefits from applied compressive strain whereas NMOS performance is supported by tensile strain. The use of this stress-engineering also implies the possibility to locally measure the stress inside the channel region. In this topic, the use and optimization of micro-Raman spectroscopy is investigated for measuring the local stress in state-of-the-art finFET transistor structures and other next-generation semiconductor architectures. Raman spectroscopy relies on inelastic scattering of photons where energy is carried away by or extracted from the crystal in the form of lattice vibrations. The student will learn to work with a micro-Raman system using different laser wavelengths. The experimental focus is on using the nanometer-scale dimension of the device to locally increase the Raman signal originating from the channel region leading to so-called nano-focused Raman, as well as the isolation of relevant information from the background using polarization considerations. Given the very complex nature of such local opto-electrical effects, simulations of the problems will be indispensable for the correct physical understanding of the experimental results. Therefore, a strong physics

background is required. The student will be trained in working with a Raman system and characterize advanced semiconductor device structures. He/she will be part of the materials and component analysis (MCA) department.

Type of project: Thesis or internship project or combination of both

Degree: Master in Science and Master in Engineering majoring in physics, chemistry/chemical engineering, electrotechnics/electrical engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Thomas Hantschel (thomas.hantschel@imec.be) and Thomas Nuytten (thomas.nuytten@imec.be).

Transmission electron microscopy: more than an image

Transmission electron microscopy (TEM) is an essential analysis technique for the development of advanced 3D semiconductor devices. It allows imaging of device structures with very high spatial resolution in different modes as well as chemical analysis of the local composition with sub-nanometer resolution. Interpretation of the images for metrology purposes is generally directly possible. However more advanced interpretation for extracting detailed (quantitative) materials properties requires further analysis of the images or spectra. E.g. strain analysis at defects and in devices can be done in several ways based on either high resolution lattice images or diffraction patterns, compositional analysis can be based on image contrasts or with X-ray or energy loss spectra, etc. For all these applications several software packages are available. The obtained results will be dependent on selected parameters and procedures in the software and may vary between different packages.
The work is focusing on the evaluation of different software packages for advanced interpretation of TEM results and application to different topics (strain, compositional analysis) making use of the vast database of TEM measurements of imec. The goal will be to determine best practices for several use cases and applications. It will require that the student obtains an excellent insight in the basics of electron beam/materials interactions and TEM image formation as well as of the materials properties that are investigated. Interest in materials and crystallography is therefore needed. The work is not focusing on software development or own use of the TEM instruments.

Ref: ImageEval ; http://en.wikipedia.org/wiki/Multislice ; http://tem-s3.nano.cnr.it/?page_id=2

Type of project: Internship project

Degree: Master in Science and Master in Engineering majoring in physics, chemistry/chemical engineering, materials engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Hugo Bender (hugo.bender@imec.be).

Chemical mechanical polishing of new materials

Chemical mechanical polishing (CMP) has become a key step in microelectronic device fabrication: In the deposition step before CMP, an overburden of material is deposited to fill structures with metal material. During CMP, this overburden is removed, removing all metal from the field area while leaving the material inside the trenches untouched (no metal loss). In order to produce faster and more powerful commercial microprocessors, 'new' challenging materials such as copper, ruthenium, cobalt, manganese and their alloys need to be polished. For Cu-barrier CMP for example, copper etching should be limited and galvanic corrosion between the copper and barrier materials needs to be minimized. In order to design a CMP process that can achieve this, the chemical reactions that occur between the materials and the CMP slurry need to be understood and controlled.

The scope of this study is to develop a CMP process for the polishing of new materials and to gain a better understanding of the mechanisms that govern this CMP process. The polishing environment is mainly controlled by two factors: the specific materials to be polished and the CMP slurry.
The type and combination of materials, the thickness as well as the deposition (e.g. chemical vapor deposition (CVD), physical vapor deposition (PVD), electroless deposition (ELD) or electroplating) and annealing method can be crucial in determining CMP performance. A (metal) CMP slurry uses oxidizers, complexating agents, inhibitors and pH adjusters to achieve a fine balance of chemical reactions that remove material at the surface while keeping corrosion under control by passivating the newly exposed surface during polishing. In this project the effect of various slurry components will be studied both during polishing on our experimental polisher and in a static slurry solution in a lab environment. Surface analysis techniques like X-ray spectroscopy (XPS), X-ray diffraction (XRD) and nano-indentation will provide the necessary extra information to understand which reactions and species are dominant at the surface. The analysis of the data will provide the understanding needed to design a model slurry which polishes the material away at a decent rate while achieving a good quality surface.
If the model slurry design experiments are successful, the efficiency of the optimized slurry will be tested on blanket and/or patterned wafers to make sure that the CMP process removes the required materials with no defectivity or dishing/erosion issues. For this analysis techniques like high resolution profilometry (HRP), defectivity analysis, resistivity and ellipsometry, scanning electron microscopy (SEM) and atomic force microscopy (AFM) can be used.

Type of project: Internship or thesis project or combination of both

Degree: Master's degree in physics, chemistry/chemical engineering, materials engineering, nanoscience & nanotechnology, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Lieve Teugels (lieve.teugels@imec.be).

Voltage control of magnetic anisotropy

Control of a magnetic bit by means of an electric field would allow operation of magnetic memories (MRAM) at much lower power levels than the present Spin-Transfer Torque MRAM (STT MRAM). The recently discovered Voltage Controlled Magnetic Anisotropy effect (VCMA) offers perspectives for such voltage control of magnetic bits and will be investigated in this project. Depending on the student's preference either experiments or modelling work can be done or a combination of both. When an electric field is applied normal to the interface of a dielectric – mostly MgO – and a ferromagnet the interfacial anisotropy of the thin film ferromagnet can be affected. This effect can give rise to the switching the anisotropy of such a thin film ferromagnet between an in-plane and out-of-plane magnetic anisotropy. At present the origin of the effect is discussed in literature and various mechanisms have been proposed to explain the observed effect. In this project the VCMA effect can be investigated experimentally. Alternatively simulation work can be done to investigate how a voltage controlled magnetic memory device can be built.

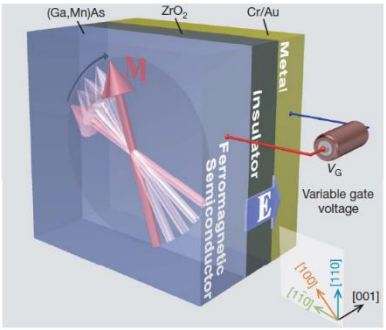


Fig. 1: Illustration of electric field control of magnetic anisotropy. From [2]

[1] T . Maruyama, Y. Shiota, T. Nozaki, K. Ohta, N. Toda, M. Mizuguchi, A. A. Tulapurkar, T. Shinjo, M. Shiraishi, S. Mizukami, Y. Ando & Y. Suzuki Large voltage-induced magnetic anisotropy change in a few atomic layers of iron Nature Nanotechnology 4, 158 - 161 (2009)
[2] D. Chiba, M. Sawicki, Y. Nishitani, Y. Nakatani, F. Matsukura and H. Ohno, "Magnetization vector manipulation by electric fields," Nature, vol. 455, p. 515, 2008.

Type of work: 10% literature, 90% experimental work and device fabrication and/or modeling

Type of project: Thesis with internship project

Degree: Master in Industrial Engineering and Master in Science and Master in Engineering majoring in physics, chemistry/chemical engineering, materials engineering, electrotechnics/electrical engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Koen Martens (koen.martens@imec.be) and Bart Vermeulen (bart.vermeulen@imec.be).

Characterization of metal corrosion in chemical solutions of different pH

In back-end of line (BEOL) processing of advanced microelectronic CMOS integrated circuits, conductor lines are made using a damascene approach by locally etching dielectric layers using plasmas through a patterned photoresist layer and filling the transferred patterns with copper. During the etching of porous dielectrics using fluorocarbon-containing plasmas such as CF4, CH2F2, and C4F8, fluorocarbon polymers are formed and deposited on the created dielectric sidewalls. These polymers (= "post-etch polymer residues" or PER) are needed to ensure etching anisotropy, profile control and to minimize dielectric degradation. However, they must be removed afterwards to achieve high adhesion and good coverage of the material (metal) deposited in later process steps in the etched features. Removal of these polymers is usually performed by a combination of a short plasma treatment and wet clean using chemical solutions or mixtures, or by wet cleans alone.

Description of the work:
The goal of this project is to study the effect of chemical solutions of different pH on the

- Corrosion of the metals and liner materials present in BEOL stacks, such as Cu, W, Co, TiN. The effect of inhibitors on metal corrosion will also be investigated.
- Possible change in properties of dielectric films, hardmask materials and etch rate of various metals and liner materials.

Main characterization techniques include:

- Inductively coupled plasma mass spectroscopy (ICP-MS) for etch rate quantification (metals).
- Four-point probe to measure sheet resistance (metals).
- Capacitance measurement to determine dielectric constant (low-k dielectrics).
- Electrochemistry (oxidation and etching kinetic).
- Spectroscopic ellipsometry (SE) to determine thickness and refractive index (certain metal oxides, polymers and dielectric films).
- Fourier transform infra-red spectroscopy (FTIR) to determine functional groups and bonding structure (polymers and dielectric films).

Type of project: Thesis or internship project

Degree: Master in Science and Master in Engineering majoring in chemistry/chemical engineering, materials engineering

Responsible scientist(s):
For further information or for application, please contact Quoc Toan Le (QuocToan.Le@imec.be) and Els Kesters (els.kesters@imec.be).

Topogolical insulator – based schemes for magnetic configuration detection

During the past few years, there has been a constant demand for smaller, faster and less power-hungry devices. As CMOS technology continues to scale down, quantum effects start to play a more important role. Furthermore, increasing demand in computation efficiency and speed have pushed research towards alternative, non-charged based technologies. An important field that is being studied thoroughly over the past few years is the field of spintronics. In comparison to the charged-based CMOS technology, where the charge of the carriers is used to define the logic states 1 and 0, in spintronics, the quantum-mechanical state of the electron's spin (up or down) is used instead. This spin orientation defines the magnetization of the material, so in essence, the role of charge is being taken over by the magnetization. This approaches can lead to faster, smaller and more robust memory devices as well as increase the capabilities of logic devices through wave computation schemes. For memory devices, the information is encoded in the magnetization texture (spin configuration) of the material whereas for logic devices, the current spintronic approach encodes the information in the spin-wave, which is a collective oscillation of electron's spins in the material. However, a basic challenge that we are currently facing is the efficient detection of such spin configurations, either time-varying (spin-waves) or non-time varying (domain walls, skyrmions, vortices). More specifically, an electrical detection is required in order to couple spin with electrical signals that we use. Consequently, research is being done towards spin-orbit coupling (SOC) materials where the spin orientation is connected with the momentum of the electron. A perfect example of such materials are Quantum Spin Hall insulators (QSH), in 2D and Topological Insulators (TI) in 3D. The strong SOC in these materials results in the spin-lock mechanism where the spin and momentum of the electron depend on each other. As a result, any change in the spin affects immediately the direction of the carriers and vice versa, thus leading to scattering. The scope of this master thesis is the study of the current schemes for electrical detection of magnetic configurations based on TI. The student should have an adequate background in quantum mechanics and solid state physics. Background in numerical methods is also desirable. Finally the student will be benefited from the in-house knowledge in the field. For further questions, do not hesitate to contact the supervising scientists.

Type of project: Thesis project

Degree: Master in Science and Master in Engineering majoring in physics, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Bart Sorée (bart.soree@imec.be) and Dimitrios Andrikopoulos (dimitrios.andrikopoulos@imec.be).

Topogolical insulator – based schemes for magnetic configuration excitation

During the past few years, there has been a constant demand for smaller, faster and less power-hungry devices. As CMOS technology continues to scale down, quantum effects start to play a more important role. Furthermore, increasing demand in computation efficiency and speed have pushed research towards alternative, non-charged based technologies. An important field that is being studied thoroughly over the past few years is the field of spintronics. In comparison to the charged-based CMOS technology, where the charge of the carriers is used to define the logic states 1 and 0, in spintronics, the quantum-mechanical state of the electron's spin (up or down) is used instead. This

spin orientation defines the magnetization of the material, so in essence, the role of charge is being taken over by the magnetization. This approaches can lead to faster, smaller and more robust memory devices as well as increase the capabilities of logic devices through wave computation schemes. For memory devices, the information is encoded in the magnetization texture (spin configuration) of the material whereas for logic devices, the current spintronic approach encodes the information in the spin-wave, which is a collective oscillation of electron's spins in the material. One of the challenges is to excite (create) such magnetic configurations. More specifically, the goal is to use electrical signals in order to affect electron's spin and reorient it in such way so as to have a stable configuration corresponding to a domain wall, skyrmion, vortex, or even a time-varying configuration corresponding to a spin-wave. Towards this end, materials that can strongly couple electron's spin and momentum are preferred. Such a coupling is found by the name spin-orbit interaction in literature and is responsible for the Quantum Spin Hall effect, where the spin and momentum of the electron are dependent on each other. One of the hottest topics in this field is the use of 3D Topological Insulators (TIs) which have high SOC and thus high efficiency in converting charge to spin. The scope of this master thesis is the study of TI as a means to excite different magnetic configurations that can be used in spintronics applications. The student should have an adequate background in quantum mechanics and solid state physics. Background in numerical methods is also desirable. Finally the student will be benefited from the in-house knowledge in the field. For further questions, do not hesitate to contact the supervising scientists.

Type of project: Thesis project

Degree: Master in Science and Master in Engineering majoring in physics, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Bart Sorée (bart.soree@imec.be) and Dimitrios Andrikopoulos (dimitrios.andrikopoulos@imec.be).

Synthesis and manipulation of large area 2D transition metal dicalchogenides

The electronic industry is progressively moving towards few-nanometer-scale CMOS and 3D IC designs. The extremely reduced dimensions of transistors make difficult a full gate-control of the current paths throughout the bulk active channel. These are called "short channel effects" which represent a serious drawback for device scaling since they can drastically degrade the operation characteristics producing also excess leakage and power consumption. How to improve the current gate-control and minimize leakages? The ideal solution could be to confine charge flow in a one atom thick layer. In this context, layered transition metal dichalcogenides (TMDs) are emerging as a new platform for exploring 2D semiconductor physics. [1-3] These consist of molecular layers stacked together by weak van der Waals interactions. Layered materials can be separated by exfoliation/delamination techniques into individual two-dimensional (2D) sheets. These materials are fundamentally different and more flexible than traditional semiconductors. In particular, the relaxed lattice matching condition permits to combine almost any layered material and create artificial heterojunctions with designed band alignment. However, synthesis of large area TMD films with clean and abrupt interfaces remain challenging and require the development of highly controllable growth and transfer processes.
The student will be involved in an experimental research activity mainly focused on 2D TMDs and related device applications.
This interdisciplinary activity combines physics, chemistry, material engineering, and nanoscience.

The experimental activity will consist in:

- transfer and characterization of TMD single layers with particular focus on interface quality
- fabrication of artificial heterostructures based on large area 2D materials
- electrical characterization of proto-device structures (FET, TFET)

[1] M. Chhowalla et al., Nat. Chem. 2013, 5, 263–275
[2] B. Radisavljevic et al., Nat. Mater. 2013, 12, 815–20, 2013
[3] D. Chiappe et al., Adv. Mater. Inter. 2015, doi: 10.1002/admi.201500635

Type of project: Thesis project

Degree: Master student majoring in physics, chemistry/chemical engineering, materials engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Daniele Chiappe (daniele.chiappe@imec.be), Cedric Huyghebaert (Cedric.Huyghebaert@imec.be) and Inge Asselberghs (Inge.Asselberghs@imec.be).

Optimization of graphene devices

Graphene, an atomically-thin sheet of carbon atoms arranged in a sp2 honeycomb lattice, has been successfully isolated for the first time only in 2004 (this achievement was awarded the Nobel prize of Physics in 2010). Ever since, new exciting reports are appearing in literature about the peculiar electronic properties of graphene, which mainly arise from the configuration of its energy band structure, combined with the intrinsically low occurrence of defects and the stiffness of its lattice, allowing for the featuring of intriguing 2-D physical phenomena.
Graphene has been proposed as a candidate for many purposes, from electrodes to CMOS and post-CMOS electronics. However, in order to make electronic applications of graphene realistic, one has to necessarily tune its electronic properties, so that, for example, a bandgap can be introduced. Another important aspect of the current graphene research entails the finding of a synthetic alternative to micromechanical exfoliation for graphene production, in order to achieve high quality, large scale graphene, addressable for CMOS-compatible device fabrication
The objective of this study is to explore new device architectures by manipulating the graphene properties targeting the specs of future technology nodes. The student will learn to handle graphene sheets, fabricate graphene FETs, and characterize their performance.
Some of the challenges involved:

1. The study of the interaction between graphene and the different active layers in the device (e.g. graphene-metal contacts, gate stack,...); by investigation of the electronic modifications of the graphene properties influenced by its environment;
2. Post-processing of graphene (e.g., transfer, device design and fabrication);
3. Electrical and/or structural characterization of (integrated) graphene devices.

Type of project: Thesis or internship project or combination of both.
This project is open to self-supporting students only (no imec allowance will be provided).

Degree: Master student majoring in physics, chemistry/chemical engineering, materials engineering, bio-engineering, electrotechnics/electrical engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Inge Asselberghs (Inge.Asselberghs@imec.be) and Dennis Lin (dennis.lin@imec.be).

Surface chemistry and electrochemistry of III-V semiconductors for atomic layer etching of high mobility channel materials

The focus of this project is on surface chemistry and electrochemistry of III-V compound semiconductors (e.g. InP, InGaAs, InAs). These materials are currently investigated as new building blocks for the realization of high mobility channels in 5-7 nm transistor devices. The integration of III-V semiconductors on existing Si platform wafers is challenging and complicated by the (very) aggressive downscaling of transistors in size. One of these challenges is the wet-chemical treatment of the surface which is needed for preparing the surface for subsequent processing steps

(e.g. prior to epitaxial growth, ohmic contact formation, dielectric deposition). As the dimensions of device structures is small, dissolution (i.e. etching) of the semiconductor needs to be highly selective and controlled at the atomic-layer-scale. Studying the dissolution kinetics of the semiconductor in various acidic media by both chemical and electrochemical methods is of critical importance. Based on the insight in oxidation kinetics, oxide solubility, charge transfer reactions, surface morphology, stoichiometry etc. a dissolution mechanisms can be proposed which can be applied for the development of highly sophisticated surface preparation strategies.
During this MSc thesis, the focus will be on the semiconductor chemistry of GaSb in acidic solution in order to resolve the basic etching mechanism (oxidation and dissolution kinetics, hydrodynamics, surface passivation, etc.). Subsequently, electrochemical methods will be used to study the importance of electrochemical processes at the semiconductor/electrolyte interface. In this case the oxidizing agent in solution (e.g. O3, O2, H2O2) removes electrons from the valence band generating mobile charge carriers (holes), which, when localized in surface bonds, can cause preferential oxidation of the group III element, leaving the group V element in the zero-valent state. The latter will induce bandgap states detrimental for device performance.
Various techniques will be used for this project:

- ICP-MS for measuring dissolution kinetics and stoichiometry, oxide formation and removal at the sub monolayer scale.
- XPS for determination of chemical bonding, surface composition and termination during etching.
- Atomic Force Microscopy for studying the surface morphology after wet-chemical treatment.
- Photoluminescence for obtaining insight in surface and interface passivation.
- Semiconductor electrochemistry (Voltammetry, Impedance measurements) for obtaining insight in dissolution mechanisms, band energetics, charge transfer reactions, etc.

Student Qualifications
We are looking for enthusiastic and motivated students with a strong interest in physical inorganic chemistry, material science, nanoscience or related field.

Type of project: Thesis project
This project is open to self-supporting students only (no imec allowance will be provided).

Degree: Master in Science majoring in chemistry/chemical engineering, materials engineering, nanoscience & nanotechnology
Responsible scientist(s):
For further information or for application, please contact Dennis van Dorp (vandorpd@imec.be).

The use and benefits of electroless deposition techniques for IC packaging applications

The use of electroless deposition techniques for IC fabrication in the back-end of line and packaging domains is of particular interest due to different reasons. Electroless techniques offer on one hand the possibility to metallize a seed metal of choice while not depositing on the surrounding dielectric (selective deposition technique). On the other hand, a metal can also be placed on a non-conductive substrate by electroless deposition when a suitable catalyst solution is applied first on the starting substrate. This last approach is of particular interest for IC packaging where metal coatings need to be placed on top of an industrially relevant laminated surface. This study will focus on the possibility to use electroless deposition to coat laminated substrates with a shortlist of metals (Ni, Cu, Co) while also evaluating/scoring the EHS aspect of the applied chemistry packages. As for the criteria of success of placing a metal film on top of a laminate material, adhesion will be investigated and a setup for peel strength measurements as well as its characterization will be established.

The benefits of the student investigating this topic will be:

- Learning all details about electroless deposition techniques and chemistries of interest
- Evaluate the EHS impact of selected chemistries (assuming further use as an actual industrial application): chemistry performance from material point-of-view vs EHS impact
- Applying this learning on coupon scale in a glovebox environment on different substrates, more particular on industrially relevant laminate materials
- Insight in characterization techniques to quantify adhesion and peel strength

Type of project: Thesis or thesis with internship project

Degree: Master in Industrial Sciences majoring in chemistry/chemical engineering, materials engineering

Responsible scientist(s):
For further information or for application, please contact Kevin Vandersmissen (Kvdsmis@imec.be) and Shashi Vyas (Shashi.Vyas.ext@imec.be).

Study of ferroelectric layers for advanced transistor design

Ferroelectricity (FE) and anti-ferroelectricity (AF) are physical phenomena that have been studied for many years for various application fields. Apart from the (already commercialized) application of ferroelectric layers in nonvolatile memories (memories that keep their information in the absence of a voltage supply), recently more effort has been put into the exploration of similar layers in steep-subthreshold CMOS transistors. Indeed, with many new applications such as e.g. the Internet of Things requiring battery, RF or even scavenging as a voltage supply, the cry-out for deep low power transistors is getting louder and louder. One way to get around the subthreshold leakage with decreasing supply voltages (the so-called Boltzmann tirany), is indeed to provide a steeper subthreshold slope. This can be accomplished by using an anti-ferroelectric gate dielectric which boosts the device transconductance in a dynamic way. Moreover, memories should preferably be nonvolatile as well in these applications as the standby and sleep mode power is then also minimized. The purpose of this thesis is to look into such materials in order to narrow down the best options for both the AF and the FE case in advanced device concepts. This includes also the use of 2D channel materials such as MX2 which are gaining a lot of interest nowadays.
The work includes literature study, evaluation of short loop experiments by electrical as well as physical analysis tools such as XRD, TEM etc. There is a team of experts to support the internship on both materials as well as electrical aspects.

Type of project: Internship project

Degree: Master in Science and Master in Engineering majoring in physics, chemistry/chemical engineering, materials engineering, electrotechnics/electrical engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Christoph Adelmann (Christoph.Adelmann@imec.be).

High quality graphene growth and transfer

Graphene is the name of a two-dimensional, one atom thick material, whereby the carbon atoms are arranged in a chicken wire type ordering. The Nobel Prize Physics was awarded to the 'inventors' of this material, as it exhibits extra-ordinary properties in terms of electrical and thermal conductivity and mechanical strength. Many high technological applications are envisioned ranging from (bio)sensors to interconnects and photonics devices.
Initially, the 'synthesis' was done by exfoliating a thin flake from a high tech pencil point, but currently a range of chemical synthesis routes are emerging. These should allow large area, defect free growth of a 2D material. Chemical vapor deposition is the most promising graphene growth technique for technological applications, due to its low cost and possible high quality large area graphene growth. During the graphene synthesis, a carbon containing gas is supplied to a substrate at high temperature. This substrate often contains a transition metal, since these metals possess a high catalytic potential for graphene growth. Nevertheless, the obtained graphene roughness, grain boundaries and control over the number of graphene layers are still a bottleneck for the implementation of CVD graphene in semiconductor applications. Some of the issues could be solved if graphene is grown epitaxial on top of a crystalline transition metal surface. Given the growth temperature and a necessity of a catalytic growth template, a direct graphene growth on electronic devices is unfeasible. Therefore, the development of a scalable transfer method is a second requirement to use graphene in electronic devices. Several transfer process possibility are documented in literature, but up to now, the graphene transfer suffers from contamination often coming from the temporary support layer and/or etching products, wrinkle formation during bonding, crack formation during graphene handling... Resolving the above issues is a must for graphene applications in emerging fields, as currently many 'demonstrations' are still done on exfoliated graphene at a lab scale. In order to achieve a successful and scalable transfer of a thin graphene layer to a target wafer, the graphene layers needs to be lifted from the growth substrate, i.e. the adhesion between both layers need to be minimized. Furthermore, the target wafer needs to be functionalized, so that the adhesion is improved and graphene doping is controlled.
To summarize, the first goal is the growth of high quality graphene layer, with a controlled number of layers and a low defect density. The second goal is to develop a reproducible and scalable transfer method, so that graphene can be integrated in electronic devices.

Type of project: Thesis project

Degree: Master in Science and Master in Engineering majoring in physics, chemistry/chemical engineering, materials engineering

Responsible scientist(s):
For further information or for application, please contact Steven Brems (Steven.Brems@imec.be) and Ken Verguts (Ken.Verguts@imec.be).

Study of reliability and variability in advanced FET devices

In order to maintain the trend of ever-increasing performance, several directions have been pursued by the semiconductor industry in the past decade. i) Conventional Si and SiO2 are being replaced by more exotic materials, from high-k gate dielectrics to metal gates and to high-mobility substrates, ii) new 3D device architectures, such as FinFETs and nanowire FETs, are being introduced, and iii) devices are downscaled toward atomic dimensions, resulting in increased device-to-device variability.
The thesis will concentrate on measurements and simulations of degradation of advanced devices (Fin and gate-all-around nanowire FETs). Since no two deeply-downscaled nominally-identical devices are the same in reality, a large number of devices needs to be characterized using semi-automatic prober stations to obtain distributions of device parameters. Modification of existing measurement routines may be required to implement adaptable measure-and-stress sequences. Large amounts of data will be generated, optionally requiring additional databasing and parameter extraction software.

Measurements will be complemented by simulations of as-fabricated (i.e., time-zero, or static) and degraded (so-called time-dependent, or dynamic) device parameter variability using state-of-the-art software employing distributed "grid" computing. The degradation can be modeled with individual gate-oxide defects, with the impact of each defect depending e.g. on the defect position (side vs. top gates), the defect energy level, the channel potential distribution induced by randomly distributed dopants and interface states, local metal work function variations, etc.
The focus of the thesis may be tailored based on the background of the applicant.

Type of work: 40% experiments, 40% modeling and simulations, 20% software development

Type of project: Thesis or thesis with internship project

Degree: Master in Science and Master in Engineering majoring in physics, electrotechnics/electrical engineering, nanoscience & nanotechnology, computer science

Responsible scientist(s):
For further information or for application, please contact Ben Kaczer (kaczer@imec.be) and Jacopo Franco (francoj@imec.be).

Investigating novel metrology concepts for the characterization of beyond silicon semiconductors

In order to continue CMOS scaling for the 7 nm node and below, the integration of advanced semiconductor materials such as Germanium (Ge) and III-V compound semiconductors (InGaAs, InAlAs) is indispensable. This is mainly due to the fact that the charge carriers inside the latter materials exhibit significantly lower effective masses and hence offer enhanced mobility and injection velocity values compared to silicon (Si). To date, Ge and III-V compound materials can be grown epitaxially on Si substrates, however, the large differences in lattice constant and material characteristics typically lead to very high defect densities in these layers. These extended defects cause a degradation of the material properties (i.e. carrier mobility) and hence device performance. As a consequence, assessing the crystalline quality of these materials (typically integrated in fin or nanowire architectures) is of utmost importance. Moreover, controlling layer parameters such as composition, strain and dimensions becomes more and more difficult but at the same time also more crucial. To address these questions, the student will therefore explore to which extend various metrology concepts like e.g. x-ray based techniques (e.g. XRD) as well as optical analysis approaches (e.g. time-resolved photoluminescence) can be used. It must be noted that especially the confined nature as well as the large surface-to-volume ratio of advanced nanostrcutures represent serious challenges for the aforementioned techniques. Hence, a careful evaluation as well as further developments (e.g. surface passivation schemes to prevent undesired excess carrier recombination in case of photoluminescenc experiments) are within the scope of this project. A part of the experimental work will be carried out in imec's state of the art 300mm cleanroom.

Type of work: 20% literature study, 60% experimental work, 20% analyzing, modeling and understanding

Type of project: Thesis or internship project or combination of both

Degree: Master in Science and Master in Engineering majoring in physics, materials engineering, nanoscience & nanotechnology, electronics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Andreas Schulze (Andreas.Schulze@imec.be).

Optical characterization of 2D transition-metal dichalcogenide semiconductors

Recently, there is a growing interest in the family of two-dimensional (2D) transition-metal dichalcogenide semiconductors MX2 (M stands for Mo or W and X stands for S, Se or Te). The most extensively studied member of this family is MoS2. The latter is an indirect bandgap material in its bulk form, however, becomes a direct bandgap semiconductor (Eg=1.88eV) when thinned to a monolayer. Such a wide bandgap and the structural similarity with graphene makes the material an interesting candidate for potential applications in logic electronics. The most common fabrication procedure for single to few-layer MX2 is mechanical exfoliation ("scotch tape method") from high-quality natural bulk MX2 crystals. However, exfoliation techniques suffer from small flake sizes and yield limitations which prevents the technique from being adopted for large scale applications. For this reason, imec is currently exploring various methods for growing high-quality large-area few-layer MX2. In order to support the development of such processes, adequate metrology capable of analyzing e.g. the layer thickness, the crystalline orientation and the layer stacking need to be provided, too. This becomes particularly challenging due to the limited volume available for probing as well as the demand for non-destructive techniques with mapping capabilities. Recently, optical second harmonic microscopy has shown great potential in characterizing mono- to trilayer MoS2 with respect to crystal orientation, domain size and layer stacking. This is possible since few-layer MoS2 (for odd numbers of layers) lacks inversion symmetry and hence allows strong second harmonic generation (SHG). Such a nonlinear optical effect can thus be used for fast and noninvasive characterization and can furthermore be applied to any substrate with weak second-order nonlinearity. Moreover, SHG could be a useful tool for monitoring material modifications which may occur during device fabrication, e.g. patterning or gate stack deposition.
The goal of this internship is to explore and understand the possibilities of optical second harmonic microscopy to study the nonlinear optical properties of MoS2 and to correlate the latter with layer properties such as thickness, orientation, layer stacking and process induced modifications. The measurements will be correlated with more established techniques such as photoluminescence and Raman spectroscopy.

Type of work: 20% literature study, 40% experimental work, 40% analyzing, modeling and understanding.

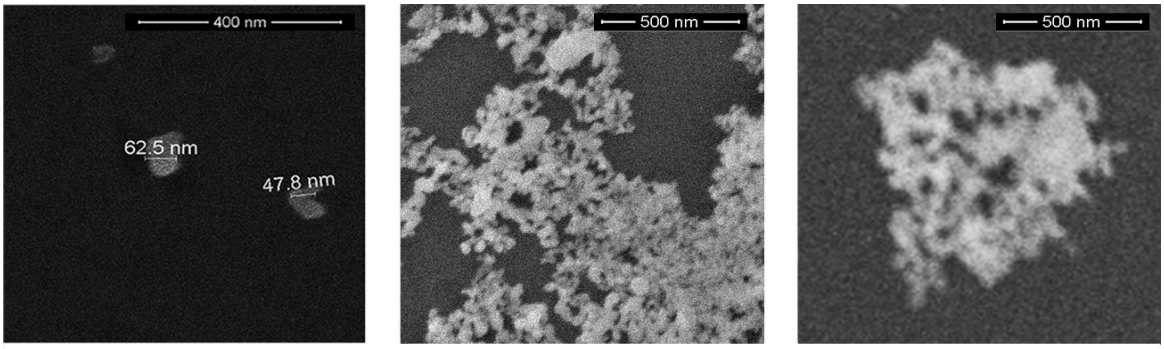
Type of project: Thesis or internship project or combination of both

Degree: Master in Science and Master in Engineering majoring in physics, materials engineering, nanoscience & nanotechnology, electronics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Andreas Schulze (Andreas.Schulze@imec.be).

Measurement of nanomaterial release during chemical mechanical planarization (CMP)

Nanostructured objects represent increasingly important products of nanotechnologies having a wide range of applications in healthcare, interconnect, biosensors etc. Such objects contain structures smaller than 100 nm in at least one dimension. Nanoparticles can be released during various processing steps and handling and may represent an occupational hazard.



The topic aims to compare risk assessment approaches currently in use in available literature. On a second place, the student will develop an assay determining the nanoparticle morphology in in the waste water from Chemical Mechanical Planarization (CMP). The experimental part will include setup development and analysis (scanning electron microscopy SEM, X-ray photoelectron spectroscopy, XPS). We are looking for a candidate with enthusiastic attitude and basic knowledge of physical chemistry, material science or nanoscience.

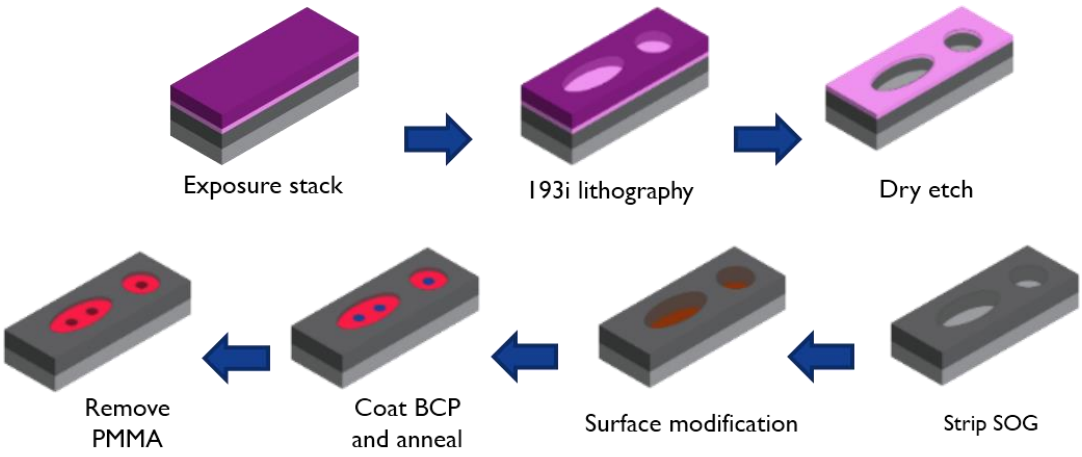
Type of project: Thesis with internship project

Degree: Master in Industrial Sciences majoring in chemistry/chemical engineering, materials engineering, nanoscience & nanotechnology

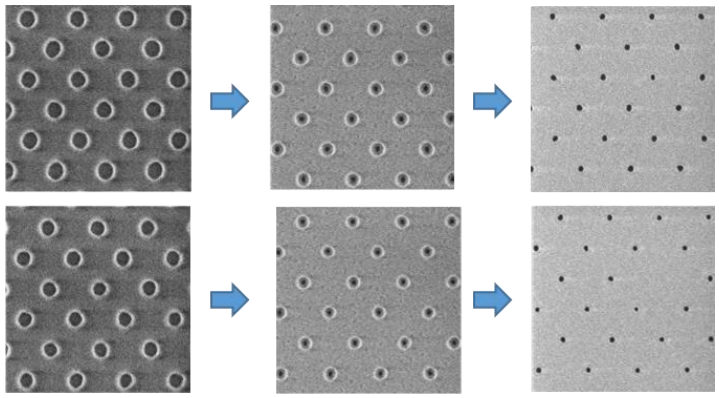
Responsible scientist(s):
For further information or for application, please contact Dimiter Prodanov (Dimiter.Prodanov@imec.be).

Contact hole shrink using directed self-assembly of block copolymers

In this project, we use a grapho-epitaxy flow for directed self-assembly (DSA) of cylindrical forming block copolymers (BCP) for contact hole shrink applications. The goal is to characterize the dimensions of the topographical structures and the subsequent fill level on BCP assembly that will allow an effective pattern transfer to layers of interest for integration.



The templated DSA process developed at imec uses 193nm immersion lithography to generate hole patterns with different critical dimensions, which are transferred into a temperature-resistant layer. The topographic features are further functionalized and a film of cylinder forming poly(styrene-b-methyl methacrylate) block copolymer is applied and annealed. After removal of the PMMA cylinders, the holes obtained with DSA of BCP are transferred into the underlying substrate stack. Previous work has shown that BCP assembly depends on the geometry of the pre-patterns. Also, the ability to transfer the DSA holes into layers of interest is closely related to the thickness (or fill level) of the polymer structure assembled in the templates.



The main focus of this work is on metrology for integration of these features into electrically functional structures. This requires characterization of the dimensions of the pre-patterns each step of the process using scanning electron microscopy (SEM) in the advanced 300mm imec wafer fab. In addition, atomic force microscopy (AFM) will be used to collect information of the fill level of the BCP inside the templates. The collected CD and profile information of the DSA structures will be correlated with their performance in the subsequent pattern transfer process in order to understand the conditions for a high performance DSA lithography process. Depending on skills and interest, wafer processing may be included in a later phase of the project.

Generic DSA literature:

1. H.S. Philip-Wong et al., Block Copolymer Directed Self-Assembly Enables Sublithographic Patterning for Device Fabrication, Proc. of SPIE Vol. 8323, 832303, 2012. doi: 10.1117/12.918312
2. W. Hinsberg et al., Self-Assembling Materials for Lithographic Patterning: Overview, Status and Moving Forward, Proc. of SPIE Vol. 7637 76370G, 2010. doi: 10.1117/12.852230

Type of project: Thesis or internship project or combination of both

Degree: Master in Science and Master in Engineering majoring in physics, chemistry/chemical engineering, materials engineering, nanoscience & nanotechnology, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Roel Gronheid (gronheid@imec.be) and Paulina Rincon (rincon@imec.be).

Defect reduction in directed self-assembly processes

With scaling of electronic devices, printing of the structures that are required to make them has become more and more complex and costly. For a few years, directed self-assembly (DSA) has been considered as a viable and low-cost alternative and complementary patterning option for keeping the down-scaling alive in the coming years, while ensuring an economic benefit to the silicon industry. DSA processes using block co-polymers to pattern uniform line-space patterns and arrays of holes with resolutions much smaller than the capability of the current lithographic nodes have been successfully demonstrated by various research/industrial groups around the globe. Several figures of merit have been identified and put forward as major checkpoints to assess the relevance of DSA processes for high-volume manufacturing environment; defectivity, roughness, placement accuracy, repeatability and robustness, cost of development and implementation being some of the important ones.
Your project will focus on one of the main factors that would make or break the show for DSA to be adopted by the IC manufacturers/production fabs – reducing the number of defects on the wafer after DSA and to be able to identify their root causes. Defects can be induced by various factors: non-ideal assembly (external and/or on-wafer) conditions, DSA material(s)-induced defects, non-DSA processes related defects (e.g. etch processes) and additionally in most cases, a cross-interaction of the above factors. One of the challenges in this study is to be able to identify/isolate the impact of the above factors on the different defect types we see after DSA. A routine part of this project will involve getting accustomed to advanced lithography tools (in our 300 mm production line environment), like immersion scanners/track clusters to define our process wafers and metrology tools like optical defect inspection, SEM-based defect review, CDSEM, optical scatterometers for characterizing and measuring defect densities of our processes and offline software packages for data analyses.
The main goal of your Masters' thesis/internship is to support and enable the defect reduction strategies of the DSA program at imec in the line-space and/or the contact hole DSA patterns, with inputs from both process improvements and running and optimizing the defect metrology. The ultimate aim of the study is to demonstrate the ability of the process to reproducibly deliver low defectivity on full 300 mm wafers. As you get familiar with the DSA process and defect inspection techniques, the focus of your study will shift more towards automated defect review/classification capabilities using a 300 mm in-line review SEM and a dedicated software platform that would reduce the need for manual defect classification, hence bringing down the data analysis duration by at least a factor 4. For this, you will leverage on the 14 nm half-pitch chemo-epitaxy DSA flow for line-space patterns developed in-house and on all the know-how about defect inspection/review strategies, both internally at imec and from external partners. A big part of your tasks will also include running the weekly defectivity monitor flow and analyzing the data from it, which acts as the baseline to assess the impact of the various defect reduction approaches we adopt.

Generic DSA literature:

1. H.S. Philip-Wong et al., Block Copolymer Directed Self-Assembly Enables Sublithographic Patterning for Device Fabrication, Proc. of SPIE Vol. 8323, 832303, 2012. doi: 10.1117/12.918312
2. W. Hinsberg et al., Self-Assembling Materials for Lithographic Patterning: Overview, Status and Moving Forward, Proc. of SPIE Vol. 7637 76370G, 2010. doi: 10.1117/12.852230

Project specific literature:

1. P. Delgadillo et al., Defect source analysis of directed self-assembly process (DSA of DSA), Proc. of SPIE Vol. 8680, 86800L, 2013. doi: 10.1117/12.2011674
2. P. Delgadillo et al., All track directed self-assembly of block copolymers: process flow and origin of defects, Proc. of SPIE Vol. 8323, 83230D, 2012. doi: 10.1117/12.916410
3. C. Bencher et al., Directed Self-Assembly Defectivity Assessment, Proc. of SPIE Vol. 8323, 83230N, 2012. doi: 10.1117/12.917993

Type of project: Thesis or internship project or combination of both

Degree: Master in Science and Master in Engineering majoring in physics, chemistry/chemical engineering, materials engineering, nanoscience & nanotechnology, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Roel Gronheid (gronheid@imec.be) and Hari Pathangi (pathangi@imec.be).

Calibration of TCAD process simulators for sub-10nm WFIN FinFET

The aggressive downscaling of FinFET devices in past years has put a great emphasis on the need to characterize two- (2D) and even three-dimensional (3D) carrier profiles for the correct understanding of device behavior. In such scaled devices even the smallest variations of the structure dimensions (ie. fin width or length, local interconnect or spacer, etc.), carrier distribution and/or activation rate can cause significant variations in the electrical properties of the devices.
As their modeling is complex with multiple calibration parameters, adequate two- and three-dimensional (2D)-characterization techniques have been identified as a necessity for process/device engineers and for the TCAD community to achieve an accurate modeling and calibration of the complex physical mechanisms for scaled devices.
To fulfill these needs, in recent years, scanning spreading resistance microscopy (SSRM), performed in high vacuum to boost its performance, has demonstrated its significance. Its sub-nanometer spatial resolution and high doping sensitivity make it unique.
Within this work the student will have :

- To utilize SSRM and its most recent mode named scalpel-SSRM (s-SSRM) to generate 2D carrier map inside sub-10nm WFIN FinFET (NB: Student will not have to perform measurements himself but well to understand the technique so that he can submit measurement requests)
- To learn how to run process and device simulations using XXX (defining the architecture, understanding the major implantation and activation models utilized,etc.)
- To test different possibilities to calibrate the TCAD process simulations using the SSRM 2D carrier maps (comparison between simulated and measured electrical junction positions, between 1D carrier profiles, between full 2D carrier maps,...)
- To evaluate the quality of the calibration realized (looking at simulated vs. measured characteristics like Ion-Ioff, DIBL, Cov,…)
- To propose modifications in the processing steps in order to improve the device performances

Type of project: Thesis with internship project

Degree: Master in Science and Master in Engineering majoring in physics, nanoscience & nanotechnology, electrotechnics/electrical engineering, computer science

Responsible scientist(s):
For further information or for application, please contact Pierre Eyben (pierre.eyben@imec.be) and Philippe Matagne (Philippe.Matagne@imec.be).

Design and expolaration of new brain-inspired circuits using Resistive RAM technology

Brain-inspired or neuromorphic computing takes the biological brain as an example for its design and operation. Recently, a very new approach on this topic was set forward by Jeff Hawkins and his company Numenta. His Hierarchical Temporal Memory (HTM) closely mimics the layout and operation principles of the brain. They also developed the so-called cortical learning algorithms (CLA) for this approach. All this information is open source. Up to now, Numenta only has a software emulation of their HTM. A hardware implementation requires an electronic device that has similar properties as a biological synapse. Recently, it has become clear that filamentary Resistive RAM (RRAM) fulfills that function. This new device is a programmable resistor and its operation relies on the growth and shrinking of a tiny conductive filament that connects two electrodes in a small capacitor. At imec, a large expertise exists on these devices and detailed models for describing their behavior are available.
Imec has now started to explore the possibilities of implementing RRAM in neuromorphic designs. In particular, several concepts of implementing the CLA of Numenta's HTM are investigated. The student's task is to design and test/simulate the analog circuit needed to implement this learning algorithm. The student should keep in mind that the RRAM is a stochastic device (just like the biological synapse), which means that only its average response is constant. The statistical properties are well understood and modeled.
The student's tasks are summarized as follows: familiarize with the cortical learning algorithm of Numenta's HTM (open source data), study the operation principles of filamentary RRAM (expertise at imec), design and/or propose CMOS mixed signal circuit concepts to implement the learning algorithm, and finally test/simulate these designs using the statistical models available.

Type of project: Thesis project

Degree: Master in Engineering majoring in nanoscience & nanotechnology, electrotechnics/electrical engineering, analog design

Responsible scientist(s):
For further information or for application, please contact Robin Degraeve (robin.degraeve@imec.be).

Plasma Functionalization of Novel MX2 Transition-Metal Dichalcogenides (TMDC)

In 2010, the Noble prize in physics was awarded for the groundbreaking experiments on mechanical exfoliation of graphene – an atomic monolayer of carbon atoms. Since that, the research interest in low-dimensional electronics raised exponentially. Graphene is mechanically very strong and has very high charge carrier mobilities, however it does not have an intrinsic bandgap and thus, it cannot be integrated as channel material in planar transistors. Few years ago, also the group of layered transition-metal dichalcogenides, the so-called MX2 materials, received attention since a transistor structure was built on exfoliated flakes. Devices built on MX2 are expected to be competitive to the ones using Silicon, especially at the technology nodes below 7 nm. A first challenge of MX2 materials is synthesis in the form of ultra-thin films on large area substrates; as a consequence imec recently spent efforts to develop 300mm deposition techniques specific to these few-layered materials. Another focus point are the challenges in the integration of these materials. Essential part of transistor structures are the metal-semiconductor contacts for source and drain contacts and the dielectric deposition on top of the material. Both issues are challenging, since the layered MX2 materials provide with their sulfur termination chemically inert surfaces, which lower adsorption of precursor molecules which negatively impact the adhesion of physically vapor deposited materials.
In this work-package, it is proposed to study the plasma functionalization of MX2 surfaces by means of low temperature plasmas in order to facilitate subsequent integration steps. This will include the screening of different plasma chemistries and different plasma parameters and their effects on the MX2 films as well as the subsequent metal and high-k deposition step.
The student will be expected to survey existing literature on MX2 plasma-surface interaction and will be trained in using standard processes for microfabrication to perform optical lithography, plasma-based patterning, and the deposition of metals and dielectrics. For the plasma treatments, imec's various state-of-the-art processing ICP, CCP,

and remote-plasma chamber can be used. Basic characterizations such as spectroscopic ellipsometry, profilometry, atomic force microscopy, x-ray reflectivity measurements, and the extraction of electrical parameters will be done by the student. More extensive film examination will be done in collaboration with imec's material characterization and analysis group.

Further information about two-dimensional material could be found here:
H. Zhang, ACS Nano, 2015, DOI: 10.1021/acsnano.5b05040.
R. Kappera, D. Voiry, S. E. Yalcin, B. Branch, G. Gupta, A. D. Mohite and M. Chhowalla, Nat. Mater., 2014, 13.
J. Yang, S. Kim, W. Choi, S. H. Park, Y. Jung, M. Cho and H. Kim, ACS Appl. Mater. Interfaces, 2013, 5, 4739–44.

Type of project: Thesis or internship project or combination of both

Degree: Master in Science or Master in Engineering majoring in physics, chemistry, materials engineering, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact J.-F. de Marneffe (marneffe@imec.be) or Markus Heyne (heyne@imec.be).

Assessment of III-V TFET for low power CMOS applications

Tunnel FET devices are promising steep slope transistors which have the potential of meeting power consumption targets for future generations of CMOS technology since they deliver steep switching characteristics and hence low power consumption. Silicon-based TFETs however suffer from low drive current and III-V materials are used to improve the drive current of the devices. Fabrication of relevant tunnel FET devices (in this case vertical nanowire type of devices) is complex. A simpler device structure to study the material quality and physics of the eventual TFET device is a diode. This project aims at studying different tunnel diode designs to better understand the behavior of the eventual tunnel FET device made out of the similar material combination.
The project involves lab work to fabricate the diodes and further electrical (and eventual physical) characterization of them.

Type of project: Internship project

Degree: Master in Industrial Sciences or Master in Science or Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact AliReza Alian (alian@imec.be), Nadine Collaert (collaert@imec.be) and Dennis Lin (dlin@imec.be).

III-V gatestacks: Investigation into defect reduction

In order to meet the ever increasing demand for faster and more performant electronics, the semiconductor industry continuously strives towards transistor size reduction , known to many as Moore's law. This scaling constantly poses new challenges and – having entered the nanometer range - the silicon based technology is slowly reaching its fundamental limits. Therefore the semiconductor industry is looking towards alternative materials that could possibly replace silicon in future electronics. One of the most prominent candidates is the class of III-V

materials, which consist of alloys between group III and V elements. These materials have already shown extraordinary electron mobilities (more than 10 times the mobility of silicon for InAs), can work at lower operating voltages (which reduces power consumption) and hold potential for future device architectures like gate-all-around field effect transistors (GAA-FETs) and tunneling FETs (TFETs).
Despite their high potential, production of high performance and reliable devices still remains an issue and hampers the large scale integration of III-V materials. Main challenges include chemical imperfections at the semiconductor-dielectric interface as well as defects (and charged sites) in the dielectric material itself. These defects cause electron trapping and scattering during device operation, resulting in a reduced performance and reliability.
The main focus of this project is to investigate the origin of these defects as well as possible treatments aimed at reducing the defect density. Given these defects originate from imperfections in the material (unsaturated bonds in the crystal/at the interface) most strategies will focus on a variety of chemical treatments aimed at saturating these bonds. These treatments include both liquid and gas phase processes, such as the use of sulfur compounds to passivate (S-terminate) the surface. Special attention should be paid to prevent any additional damages that might result in degradation of the material's properties and consequently degradation of the resulting device. This should improve device performance and reliability, bringing III-V materials one step closer to integration in future technology.
During this project the student will have the opportunity to perform research in imec's state-of-the-art cleanrooms and will have access to a wide variety of characterization techniques (both physical and electrical). Imec is generally considered as one of the world leaders in semiconductor research, and the student will have the opportunity to work together with many experts in their respective fields. The student will be able to make a contribution to advancing the field of III-V semiconductors.
All necessary trainings will be provided by imec. The specific focus of the project can be adjusted depending on the students interests and background. Ideally the student should be a motivated, eager to learn individual with an interest in semiconductors, surface/interface chemistry and material engineering.
During this internship the student will not receive any financial compensations from imec for his/her work.

Type of project: Internship project

Degree: Master in Industrial Sciences or Master in Science or Master in Engineering majoring in chemistry/chemical engineering, materials engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Dieter Claes (dieter.claes@imec.be).

Exploratory devices for nonvolatile, low power, and ultrafast magnetic memories

There is considerable interest in electrically controlling nano-magnets (*Spintronic*) in order to develop non-volatile magnetic memories (*MRAM*) [1]. Indeed, the microelectronics industry is facing major challenges related to the volatility of *CMOS* cache memory elements (usually *SRAM* and *eDRAM*). Due to decreasing devices size, leakage current in standby mode are now dominating the power dissipation of *CMOS* circuits. Furthermore, the increased density and reduction in die area lead to heat dissipation and reliability issues. Integration of non-volatility in memory hierarchy would solve these issues by incredibly minimizing static power consumption. *MRAMs* are among most credible candidates that are low power and fast enough to compete with *SRAM* and replace them at cache level. Most advanced MRAM devices are magnetic tunnel junctions (MTJ) that consist of two ferromagnetic layers separated by a very thin oxide barrier, one of the layer being the storage layer, the other is used as reference layer. Depending on the relative orientation of the magnetization of these two layers (parallel/ anti-parallel), the MTJ cell will exhibit low/high resistance through the tunnel magneto-resistance effect (TMR), defining the reading state (0/1). The writing operation relies on *Spin Transfer Torque* (STT)[1], which is the transfer of spin angular momentum from the reference layer to the free layer that in the end can switch reversibly the storage layer between two stable states (defined by its magnetic anisotropy). Though, *STT-MRAM* requires to inject large current across the oxide barrier for writing, which results in reliability and endurance issues at very fast operations, while it is a critical aspect for *SRAM* and *DRAM* replacement.

Spin-Orbit Torque (SOT)[2,3] is an alternative spin current source originating from the spin-orbit interaction and mediated by Spin Hall[4] and Rashba[5] interactions. SOT distinguishes by offering the possibility to switch magnetization using in-plane currents[2], unlike STT that requires a current flow in the perpendicular direction through MTJ. That allows for decoupling reading (TMR) and writing (SOT) path and this novel 3-terminal geometry naturally solves the oxide barrier breakdown issue of the *STT-MTJ*. The proof of concept of such *SOT-MRAM* was recently confirmed[6], and robust deterministic magnetization reversal at sub-ns scale was demonstrated[7]. *SOT-MRAM* seem therefore a promising solution for SRAM replacement in cache memory, even though some challenges have to be tackled before full integration in future technology nodes can be envisaged.

Work description:

i. Characterization of magnetic properties and SOT amplitude in deposited layers in order to identify best materials for realizing *SOT-MTJ*

ii. Fabrication of simplified SOT devices in order to estimate switching current densities of deposited materials and to demonstrate new concepts for realizing field-free switching at low current density.

iii. Characterization of 300mm integrated *SOT-MTJ* cells in order to benchmark their performances and demonstrate their potential for replacing SRAM in cache memory.

The work is part of the *Exploratory memory project* of IMEC. It has ambitious objectives, and will require to cover a broad area of competences: fundamentals of magnetism, spintronic and SOT physics as well as structural, magnetic and transport properties of studied stacks. The applicant should therefore have a strong interest and motivation to understand the underlying physics, keeping the application in mind.

[1] C. Chappert et al., Nature Material (2007), [2] M. Miron et al., Nature (2011); [3] K. Garello et al., Nature Nanotech (2013); [4] V.I. Perel et al., JETP Lett (1971); [5] Rashba et al., JEPT (1984); [6] M. Cubucku et al., APL (2014); [7] K. Garello et al., APL (2014)

Type of work: Electrical characterization(60%), nano-fabrication (30%), literature (10%)

Type of project: Thesis or internship project (duration minimum 6 months)

Degree: Master in Science or Master in Engineering majoring in physics, nanoscience & nanotechnology or similar

Responsible scientist(s):
For further information or for application, please contact Kevin Garello (kevin.garello@imec.be).

Characterize the patterning behavior of a soft line encapsulated in a thin layer of different stress and after exposure to various treatments

Year after year, the semiconductor industry overcomes a tremendous amount of technical challenges to satisfy Moore's law. Through innovative device architectures, smart design, new integration and patterning concepts, better tools and new materials, the industry has successfully reached the 7-nm technology node. Both design and patterning options are identified and the High Volume Manufacturing (HVM) readiness is expected end of 2018. Today, the industry is preparing for the 5-nm technology node while research centers start identifying and exploring the different patterning options for the 3-nm technology node. The former targets a Metal Pitch (MP) of 32-nm and a Contacted Poly Pitch (CPP) of 42-nm while the latter aims for a MP of 24-nm and a CPP of 32-nm. At such tight metal pitches, a significant part of the Edge Placement Error (EPE) budget will be consumed by many local and global variabilities like overlay, CD (Critical Dimension) non-uniformity, Line Edge Roughness (LER) and Line Width Roughness (LWR). Hence, the reduction of such variabilities is becoming key to enable the most advanced technologies.
The goal of this project is to study the patterning behavior of a soft line (photoresist, amorphous carbon, Spin-on carbon, polymer) encapsulated in a thin layer of different stress (varying from tensile to compressive) and after exposure to various treatments. In the first phase of this work, the student will characterize the roughness of the line before and after the aforementioned processing. In the second phase of the work, the student will do a step by

step characterization of the pattern during its transfer into the underlying layers. Finally, we will intentionally change the mechanical properties of the underlying materials and characterize the impact at pattern level with the same characterization techniques. Thin film thickness, stress, surface roughness will be characterized using ellipsometry, surface scattering technique and surface profiling techniques like Atomic Force Microscopy (AFM) and optical profiler. The PR line roughness, the CD and CD uniformity will be measured from top down SEM imaging. For both blanket and patterned roughness data, the different contributors to the roughness will be determined from a Power Spectral Density (PSD) analysis.

Type of project: Internship project

Degree: Master in Industrial Sciences or Master in Science or Master in Engineering majoring in physics, chemistry, nanoscience & nanotechnology, materials engineering

Responsible scientist(s):
For further information or for application, please contact Frederic Lazzarino (frederic.lazzarino@imec.be), Sara Paolillo (sara.paolillo@imec.be) and Stefan Decoster (stefan.decoster@imec.be).

193i SAQP versus EUV SADP at 12nm half-pitch: Performance comparison and enhancement through both stack and integration optimization

Year after year, the semiconductor industry overcome a tremendous amount of technical challenges to satisfy Moore's law. Through innovative device architectures, smart design, new integration and patterning concepts, better tools and new materials, the industry has successfully reached the 7-nm technology node. Both design and patterning options are identified and the High Volume Manufacturing (HVM) readiness is expected end of 2018. Today, the industry is preparing for the 5-nm technology node (N5) while research centers start identifying and exploring the different patterning options for the 3-nm technology node (N3). The former targets a Metal Pitch (MP) of 32-nm and a Contacted Poly Pitch (CPP) of 42-nm while the latter aims for a MP of 24-nm and a CPP of 32-nm. At such tight pitches, Spacer Defined Multiple Patterning (SAMP) is required to enable 12-nm Line/Space (L/S) grating. The first approach consists of doing a standard Spacer Assisted Double Patterning (SADP) associated to EUV lithography where the second consists of doing a Spacer Assisted Quadruple Patterning (SAQP) combined with 193 immersion lithography. The goal of the project is to compare both approaches and improve them by either engineering the stack or changing the integration scheme. The comparison will be done using top down SEM measurement (Critical Dimension (CD), CD uniformity, Line Edge Roughness (LER), Line Width Roughness (LWR)), by doing step-by-step Power Spectral Density (PSD) analysis to identify the different roughness contributors and by evaluating in all cases the Edge Placement Error budget.
In the first phase of this work, the student will focus on the comparison of both approaches using front-up stack and conventional integration. In a second phase, different stacks and integrations will be investigated. Finally, the student will establish a scorecard benchmarking all studied approaches.

Type of project: Thesis or internship project

Degree: Master in Industrial Sciences or Master in Science or Master in Engineering majoring in physics, chemistry, nanoscience & nanotechnology, materials engineering

Responsible scientist(s):
For further information or for application, please contact Frederic Lazzarino (frederic.lazzarino@imec.be) and Stefan Decoster (stefan.decoster@imec.be).

Study and understand photoresist smoothening mechanisms observed during different plasma treatments

Year after year, the semiconductor industry overcomes a tremendous amount of technical challenges to satisfy Moore's law. Through innovative device architectures, smart design, new integration and patterning concepts, better tools and new materials, the industry has successfully reached the 7-nm technology node. Both design and patterning options are identified and the High Volume Manufacturing (HVM) readiness is expected end of 2018. Today, the industry is preparing for the 5-nm technology node while research centers start identifying and exploring the different patterning options for the 3-nm technology node. The former targets a Metal Pitch (MP) of 32-nm and a Contacted Poly Pitch (CPP) of 42-nm while the latter aims for a MP of 24-nm and a CPP of 32-nm. At such tight metal pitches, a significant part of the Edge Placement Error (EPE) budget will be consumed by many local and global variabilities like overlay, CD (Critical Dimension) non-uniformity, Line Edge Roughness (LER) and Line Width Roughness (LWR). Hence, the reduction of such variabilities is becoming key to enable the most advanced technologies.
The goal of this project is to characterize the effect of different cures (different chemistries and different parameters) generated using conventional but also unconventional plasma reactors on both patterned and blanket photoresist (PR) wafers. The student will have to compare the observations made on blanket and on patterned wafers and established any existing link between both. Trimming effect and etch rates, stress, surface roughness and chemical modification of the PR will be characterized using ellipsometry, Fourier transform infrared spectroscopy, X-Ray photoelectron spectrometry and atomic force microscopy. The PR line roughness, the CD and CD uniformity will be measured from top down SEM imaging and the different contributors to the roughness determined from a Power Spectral Density (PSD) analysis.

Type of project: Thesis or internship project

Degree: Master in Industrial Sciences or Master in Science or Master in Engineering majoring in physics, chemistry, nanoscience & nanotechnology, materials engineering

Responsible scientist(s):
For further information or for application, please contact Frederic Lazzarino (frederic.lazzarino@imec.be), Sara Paolillo (sara.paolillo@imec.be) and Antony Peter (anthony.peter@imec.be).

Characterize physical properties of thin films composing an SAQP stack and study the impact during pattern transfer

Year after year, the semiconductor industry overcomes a tremendous amount of technical challenges to satisfy Moore's law. Through innovative device architectures, smart design, new integration and patterning concepts, better tools and new materials, the industry has successfully reached the 7-nm technology node. Both design and patterning options are identified and the High Volume Manufacturing (HVM) readiness is expected end of 2018. Today, the industry is preparing for the 5-nm technology node while research centers start identifying and exploring the different patterning options for the 3-nm technology node. The former targets a Metal Pitch (MP) of 32-nm and a Contacted Poly Pitch (CPP) of 42-nm while the latter aims for a MP of 24-nm and a CPP of 32-nm. At such tight metal pitches, a significant part of the Edge Placement Error (EPE) budget will be consumed by many local and global variabilities like overlay, CD (Critical Dimension) non-uniformity, Line Edge Roughness (LER) and Line Width Roughness (LWR). Hence, the reduction of such variabilities is becoming key to enable the most advanced technologies.
The goal of this project is to characterize the physical properties of the thin films composing a Spacer Assisted Quadruple Patterning (SAQP) stack and study their impact on CD and on line roughness during a step-by-step pattern transfer. In the first phase of this work, the student will set-up the metrology methodology and then characterize the different layers (first individually and then during stack formation). In the second phase of the work, the wafers will be processed following imec's standard SAQP flow. The student will have to do a step by step characterization of the pattern transfer during this SAQP process and establish a link with what was observed on blanket wafers. Finally, in order to highlight a possible correlation between film and line roughness, we will intentionally play on film roughness and characterize the impact at pattern level with the same characterization

techniques. Thin film thickness, stress, surface roughness will be characterized using ellipsometry, surface scattering technique and surface profiling techniques like Atomic Force Microscopy (AFM) and optical profiler. The PR line roughness, the CD and CD uniformity will be measured from top down SEM imaging. For both blanket and patterned roughness data, the different contributors to the roughness will be determined from a Power Spectral Density (PSD) analysis.

Type of project: Thesis or internship project

Degree: Master in Industrial Sciences or Master in Science or Master in Engineering majoring in physics, chemistry, nanoscience & nanotechnology, materials engineering

Responsible scientist(s):
For further information or for application, please contact Frederic Lazzarino (frederic.lazzarino@imec.be), Sara Paolillo (sara.paolillo@imec.be) and Stefan Decoster (stefan.decoster@imec.be).

II. GaN Power Electronics

Probing the electrical properties of next-generation III-V materials using Scanning Probe Microscopy

III-V semiconductors (GaN, InP, GaAs and their combinations) are considered as the 2nd most important material group after Si. After several decades of intensive research efforts, they have nowadays been adopted as the fundamental active material in LEDs and lasers. In the meantime, GaN, for instance, showed huge potential in power electronics applications for high voltage and high frequency switching due to their wide bandgap and their high stability. The industrialization of GaN power technology is imminent, yet some important challenges still need to be addressed. A main challenge lies in the direct electrical characterization of the device stack. Typically, the devices are grown using various III-V layers which are optimized and tuned in order to get the maximum performance in the final device. Direct electrical characterization of these layers is therefore key to advance the technology as it can provide direct input for the epitaxy process and the device design.
Scanning probe microscopy (SPM) is the ultimate tool to analyze physical and electrical properties at the nanoscale, and the aim of this internship/master thesis topic is to apply SPM based methods (such as Scanning Capacitance, Kelvin Probe Force, and Scanning Spreading Resistance Microscopy) to measure the electrical properties of III-V stacks, interpret the data and correlate the obtained results with the final device performance. In practice the student will be extensively trained in SPM methods and is expected to measure, analyze and report the obtained data in collaboration with the team members.

Type of project: Thesis of internship project or combination of both

Degree: Master in Industrial Engineering and Master in Science and Master in Engineering majoring in physics, materials engineering, electrotechnics/electrical engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Kristof Paredis (Kristof.Paredis@imec.be), Ming Zhao (ming.zhao@imec.be) and Umberto Celano (umberto.celano@imec.be).

III. Wearable Health Monitoring

Psychophysiological stress detection in a semi-controlled environment

Psychological stress is a worldwide growing problem. Currently the gold standard to measure stress is by using questionnaires. These are however just a snapshot, devious and subjective. To tackle this problem over the last years the focus of research has shifted towards physiological stress detection. Which is an objective measure, that can be monitored continuously. The goal is to measure stress by measuring physiological signals such as heart rate, skin conductance, temperature, etc.
Research has already indicated that psychophysiological stress detection in a controlled environment, i.e. the laboratory, is possible. In an ambulant environment however, this remains a difficult task since multiple factors besides stress can influence physiology, e.g. physical activity. Therefore imec has collaborated in the past with a television program to collect physiological data in a semi-controlled environment. The dataset exists of heart rate signals and corresponding video images during the program. The goal is to link these heart rate signals with the participant's stress level.
In this thesis work, first a scan of the state of the art (literature) on psychophysiological stress detection will be done. Then the aim is to first annotate the video images to identify stressful and non-stressful periods per participant. Second a model should be developed that links these annotations with the measured heart rate.

Type of project: Internship project

Degree: Master in Industrial Sciences and Master in Engineering majoring in bioscience engineering, computer science, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Walter de Raedt (deraedt@imec.be) and Elena Smets (elena.smets@imec.be).

Analysis and fusion of wearable sensor data

Microsystem technologies are currently stimulating the development and deployment of personal body area networks. These wireless networks provide lifestyle, assisted living, sports or entertainment functions for the user, without visible interference with their active lives. Prevention rather than detection and cure will be the future paradigm.
In imec's Wearable Health program, such body area networks (BAN) with several different types of sensors are currently under development: ECG signals, skin conductance, ions in sweat, motion and many more signals can be monitored, recorded and wirelessly transmitted to a hub during longer periods of time.
With the growing availability and acceptance of these sensor networks for improving our life quality, it is becomes attractive to use their information in a multitude of applications where the user can directly benefit from this information by managing his lifestyle and health.
However combining information for several sensors can reveal new insights in different domains such as healthy behavior stimulation, assisted living, stress management. Specific challenges are:

- Analyze cross platform sensor data (i.e. data from different types of sensors, such as a mix of commercial and research devices) simultaneously over large timeframes
- Search for correlations between data of these sensors (e.g. heart beat with skin conductance data for stressed people)
- Identify valid sensor data in long time series
- How to summarize the multitude of data in order to give a proper feedback message to the user?
- ...

In this thesis work, first a scan of the state of the art (literature) on sensor data management will be done. Furthermore it is then the aim to elaborate a strategy for a flexible analysis and markup (data cleaning and correlation) tool for heterogeneous sensor data for use on a pc, a mobile device and in the cloud. In a first step available captured data will be used to map sensor data from different sensors and correlate these data from different sensors: hearth rate, accelerometer data and skin conductance data will be studied over long time periods (days) searching for strategies to summarize extracted information in a clear and attractive way for the user. Next steps will then increase complexity by fusion of data from a more heterogeneous set of sensors.

Type of project: Internship or thesis project

Degree: Master in Industrial Sciences and Master in Engineering majoring in bioscience engineering, computer science, electrotechnics/electrical engineering,

Responsible scientist(s):
For further information or for application, please contact Walter De Raedt (deraedt@imec.be) and Elena Smets (elena.smets@imec.be).

IV. Life Science

Exploring distributed implementations of matrix factorization-based machine learning algorithms

Recommender Systems have become very common in recent years and are useful in various real-life applications. The most popular ones are suggestions for movies on Netflix and books on Amazon. They can, however, be used in more unlikely areas such drug discovery where a key problem is the identification of candidate molecules that affect proteins associated with diseases.
Matrix Factorization techniques such as BPMF* are among most used approaches for the design of recommender systems. These methods are very difficult to parallelize because of the size and the sparsity of the matrix and the data dependencies. The goal of this internship is to design and implement parallel distributed matrix factorization-based machine learning algorithms.
This internship will take place in imec in Leuven, Belgium. The student will be part of the Exascience Life Lab** which is a collaboration between members from the pharmaceutical industry, the technology industry, and the research sector. The Exascience Life Lab researches the application of High Performance Computing to problems in the life sciences and associated industries. We take a vertical approach, bridging from application experts with demanding performance requirements down to next generation computer architectures, via numerical algorithms and advanced programming models.

* https://www.cs.toronto.edu/~amnih/papers/bpmf.pdf
** http://www.exascience.com

Objectives:

- Identify the limitations of existing algorithms.
- Design and implement new solutions for distributed matrix factorization machine learning algorithms.
- Deploy and run multiple cutting-edge industry platforms for data processing such as SPARK, MPI, etc.
- Work with large-scale infrastructures: high-performance infrastructures (supercomputers) or cloud toolkits.
- Perform benchmarks using real data and write technical reports.

Prerequisites:

- Interested in programming parallel and distributed algorithms.
- Experience in working with Python or Java.
- Experience in working with Spark and/or MPI is a big plus.
- Basic understanding of cluster computing paradigm and supercomputers.
- Knowledge of batch scripting.
- Good professional English.
- Good interpersonal skills, team-work spirit and independent working capability.

We offer you the chance to participate in a very dynamic working environment within imec and have broad context and contact with people from the research and industrial community.

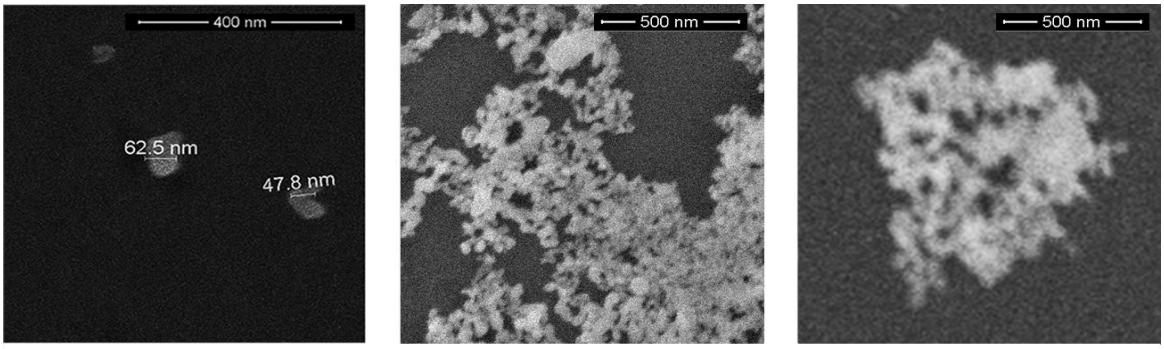
Type of project: Internship project

Degree: Master in Science and Master in Engineering majoring in computer science

Responsible scientist(s):
For further information or for application, please contact Imen Chakroun (imen.chakroun@imec.be) and Roel Wuyts (roel.wuyts@imec.be).

Automatic classification of textures and objects at the nanoscale

Nanostructured objects represent increasingly important products of nanotechnologies having a wide range of applications in healthcare, interconnect, biosensors etc. Such objects contain structures smaller than 100 nm in at least one dimension. Nanoparticles are small enough to slip into the human bloodstream and even through the walls of cells. That's made them a major source of health-related concern, but treated properly, they could also improve health.



The topic aims to develop objective and automatic approaches of image analysis of TEM images. The student will benefit from the existing expertise in image and morphological analysis in the group and is expected to develop an approach based on a combination of machine learning and image analysis approaches. Experience in machine learning and programming in Java or R is desirable.

Type of project: Thesis with internship project

Degree: Master in Science and Master in Engineering majoring in bioscience engineering, computer science

Responsible scientist(s):
For further information or for application, please contact Dimiter Prodanov (Dimiter.Prodanov@imec.be).

Ultra-fast vapor bubble jet flow cell sorting

Cell sorting is a very important sample pretreatment step for many bio-analytical applications. Not only does it provide cell counts for different species in the crude sample, the sorted thus purified cell species are important for downstream diagnosis and therapy. For example, circulating tumor cells (CTCs) can be sorted out from other white blood cells (WBCs) for cell genotyping so as to guide personalized medication to stop cancer metastasis. Imec has developed a high speed cell sorter platform where cell sorting takes place in a microfluidic chip in contrast to bulky traditional cell sorters. The key element of the cell sorter is a micro heating element which fires micro vapor bubbles and consequently a rapid jet flow that sorts cells. (Details can be found from: http://cyto.tinyfluidix.com/?p=162).
The main focus of this thesis is to study the thermodynamics of the vapor bubble growth and jet flow mechanism by physical analysis and computer thermal/fluidic finite element modeling (70% of total time). This would facilitate the development of the next generation cell sorter. The modeling will be cross verified by existing or new experimental data (30% of total time).

Type of project: Thesis project

Degree: Master in Science and Master in Engineering majoring in physics, materials science, bioscience engineering, mechanical engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Koen de Wijs (koen.dewijs@imec.be) and Chengxun Liu (chengxun.liu@imec.be).

Characterization of the effect of nano-engineered surfaces on cardiac cell maturation

Cardiotoxicity is one of the major causes of the withdrawal of drugs and termination of drug development. Despite extensive toxicity screening during drug development, current methods still offer poor predictability. These tests are generally based on cell lines or animal cardiac cells which show large genotypic difference from the human heart. A more relevant cell model consists of differentiated human pluripotent stem cell-derived cardiomyocytes (HIPSC), but these still show large phenotypical differences from adult human cardiac tissues. These cells show a more isotropic shape, unlike the elongated cardiac cells present in the human heart.
In order to structure the growth of cardiac monolayers into a more relevant system, it is possible to use biological and physical patterns. In the latter case, nanotopographic cues (such as cones and grooves) can be structured onto substrates and influence both the structure and function of cardiac monolayers. So, in order to create a more relevant heart-on-chip model, imec has developed a new microelectrode array chip with nano-engineered surfaces. This project involves characterizating the effects of the nano-engineered surface on the growth of cardiac monolayers. Cardiac cell growth will be assessed by immunohistochemical stainings, calcium imaging and electrophysiological measurements. The candidate should have a strong biological background and insight into electrophysiologal methods.

Type of project: Thesis or thesis with internship project

Degree: Master in Science majoring in biology, biomedical engineering, biomedical sciences

Responsible scientist(s):
For further information or for application, please contact Thomas Pauwelyn (thomas.pauwelyn@imec.be), Dries Braeken (dries.braeken@imec.be) and Veerle Reumers (veerle.reumers@imec.be).

Single cancer cell characterization using high-density microelectrode array

Cancer research literature has increased dramatically over recent decades due to increasing knowledge in molecular biology and genetics of the disease. However, current experimental methods are mostly performed on relatively large populations of cells obscuring the large heterogeneity in cancer cells, even within single solid tumor samples. The ability to analyze cells with single-cell precision is crucial for the investigation of rare cell subpopulations within tumors and could over time result in the development of improved cancer therapeutics.
In recent years, imec developed an advanced CMOS microelectrode array chip to analyze single cancer cells using electrical impedance spectroscopy. This technique is based on fundamental electrical properties of biological cells and can be used for cell characterization, cell status monitor and drug screening in heterogeneous cell populations. The purpose of this research project is to investigate differences in the impedance spectra of cancer cell lines and statistically process these results in order to gain knowledge about the biology of different cancer cell lines.
The research project consists partly of experimental work done in the lab and party of data processing. Data analysis is of major importance in this research project, since differences in these impedance spectra are typically small. Artificial neural networks have been used recently to distinguish different cell lines, but other machine learning techniques can be applied if these yield a better results. Data (pre-)processing and statistical analysis have traditionally been performed using MATLAB, but Python or R could also be used if preferred by the student.

Type of project: Thesis project

Degree: Master in Industrial Sciences and Master in Science and Master in Engineering majoring in biomedical engineering, biomedical sciences, bioscience engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Carl Van Den Bulcke (carl.vandenbulcke@imec.be), Dries Braeken (dries.braeken@imec.be) and Chengxun Liu (chengxun.liu@imec.be).

Nano-photonic structures to collect and enhance fluorescence emission on a SiN platform

Silicon photonics has become one of the most promising photonic integration platform in the recent years. The combination of high-index-contrast and compatibility with CMOS processing technology made it possible to use the electronics fabrication facilities to make photonic circuitry. There has been a tremendous interest towards integration of photonic devices in biological sensing and detection recently. The visible and very-near-infrared (500-950 nm) wavelength window is of great interest for this kind of applications due to low photo damage and availability of low cost sources-detectors. Unlike Silicon (Si), Silicon Nitride (SiN) is transparent in this Visible & Near-Infrared window and provides the combination of high-index-contrast and compatibility with CMOS processing technology. A low-loss silicon nitride platform has been developed here and by an extensive materials study in the 200 mm line of imec, the propagation losses were reduced below 0.5 dB/cm in visible wavelength.
For ultimate integrated fluorescence based biosensing applications, the development of devices that efficiently both excite and collect fluorescence from dyes located near the chip surface is of paramount importance. In this work, the aim is to investigate the effect of different nano-photonic structures on the fluorescence emission of the dyes residing in the near field of the structures. This investigation will help to develop nano-photonic devices to enhance the fluorescence emission and collect that efficiently by the chip.
The student will use FDTD simulation to optimize the design for structures like waveguides, ring resonators and linear resonators. Then (s)he will fabricate them using electron beam lithography. Finally, (s)he will investigate the influence of those structures on the fluorophore placed in the near field. The student will gain hands-on experience with optical experiments. Sample preparation will be handled by the student in the imec III-V cleanroom in cooperation with the daily advisor. The student will obtain experience in optical and electron beam lithography and master various deposition and etching techniques. Further sample characterization will be done by optical microscopy, scanning electron microscopy and waveguide transmission spectroscopy. The candidate should have a strong interest in photonics and nanofabrication.

Type of project: Thesis project

Degree: Master in Science and Master in Engineering majoring in physics, chemistry/chemical engineering, materials engineering, bioscience engineering, nanoscience & nanotechnology, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Md Mahmud-Ul-Hasan (Mahmud70@imec.be).

A spectroscopic glance in our daily life

How wonderful would it be, if our smartphones or smartwatches had a built-in sensor that allows us for example to check for food quality or to check for toxic substances in children's toys, etc? Raman spectroscopy could be a powerful analytical technique to identify these chemical substances by their molecular fingerprint. At imec, in the life science department, we are developing a miniaturized Raman spectrometer for this purpose. Despite the great potential of Raman spectroscopy, the techniques also has its disadvantages. For example, the presence of a fluorescent background can compromise the quantitative prediction capabilities. Hence it is critical to obtain a Raman spectrum free of such a background. There are various methods to correct for this. These methods can be separated into four categories: algorithm-based baseline correction methods, sampling optics and geometries, time gating methods, and shifted excitation methods. In this project we would like to explore some of the options in a particular case study. To do this, at imec we have several commercial Raman systems that can be adapted for these experiments.
We are looking for a master student which has a strong interest in optical characterization, interpretation and implementing algorithm-based methods to improve quantitative predictions based on Raman spectroscopy.
This project will enable the fabrication of Raman spectrometer that allow for low-cost integration in lab-on-a-chip systems by benefiting from CMOS scaling, ultimately resulting in a truly innovative, high-end life science application.

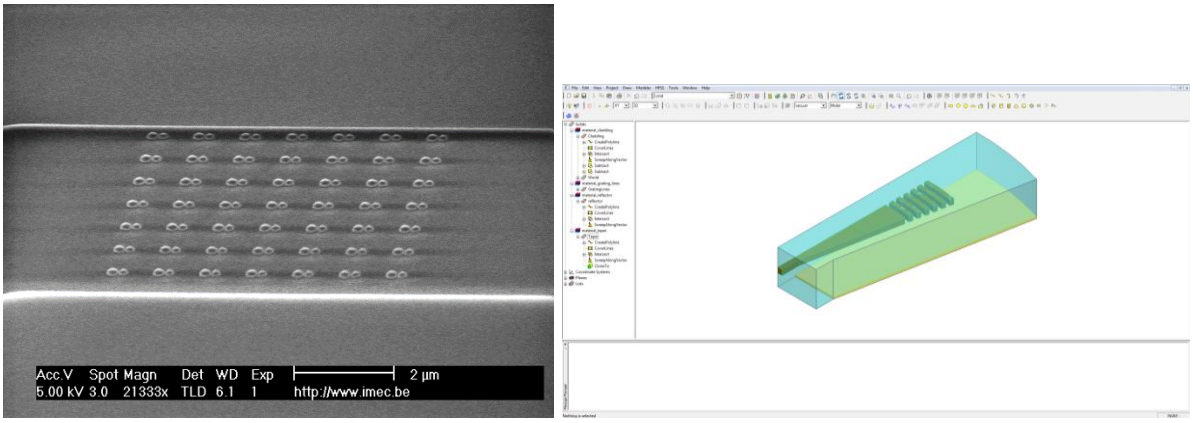
Type of project: Thesis project

Degree: Master in Science and Master in Engineering majoring in physics, chemistry/chemical engineering, materials engineering, bioscience engineering, mechanical engineering, nanoscience & nanotechnology, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Chang Chen (Chang.chen@imec.be), Pol Van Dorpe (Pol.vandorpe@imec.be) and Hilde Jans (Hilde.Jans@imec.be).

Nanophotonic phased array

Photonics, the science of generating and/or processing light waves on a micrometer-scale, is enabling evermore applications, including LED-lightning, fiber-to-the-home internet, solar panels, displays and image sensors. Recent progress in nano-fabrication now also allow to produce large-scale photonic circuits on wafer-scale using the infrastructure of the electronics industry, providing cost-effective high-quality optical systems. Imec is playing a crucial role in the development of wafer-scale photonics, and already developed a state-of-the-art silicon photonics platform for high-speed optical communication and sensing (Fig.1). Recently, we started developing an additional silicon nitride platform for photonics for visible wavelengths targeting applications in industrial and biomedical sensing.
Antenna arrays, consisting of many antennas organized in a matrix and fed with control of phase and amplitude, allow to shape and steer a beam of electromagnetic radiation, and are well-known for high-end RADAR-applications. Their counterparts in optics, photonic phased arrays, are still in development and would allow a multitude of applications, such as LIDAR (RADAR with light) for driverless cars, dynamic optical trapping of biological cells for medical diagnostics and adaptive wireless optical communication. A team at MIT successfully demonstrated a photonic phased array with infrared wavelengths [1], proving the feasibility of this component. However, wide-angle beam steering and shaping or operation at short wavelengths has not yet been shown.
Therefore, imec is also taking up the challenge to develop performant and low-cost photonic phased arrays for a plurality of applications. This thesis or internship gives you the possibility to contribute to the design and characterization. Since one of the main challenges is developing a manufacturable antenna element that allows tuning the phase and amplitude, the emphasis will be on designing and exploring compact photonic antennas.



Left: Example of photonic nano-antennas made in the imec-clean rooms
Right: Example design environment for photonic antennas

Your challenges:

- Design and compare different compact photonic antennas
- Design a phased array based on the antenna you designed
- Characterize phased arrays in the lab

This project is your chance to learn about different aspects of (photonic) chip development in an application-oriented environment.

[1] Sun, J., Timurdogan, E., Yaacobi, A., Hosseini, E. S., & Watts, M. R. (2013). Large-scale nanophotonic phased array. Nature, 493(7431), 195–9. doi:10.1038/nature11727

Type of project: Thesis or internship project or combination of both

Degree: Master in Science and Master in Engineering majoring in physics, nanoscience & nanotechnology, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Tom Claes (tom.claes@imec.be), Kristof Lodewijks (Kristof.Lodewijks@imec.be) and Xavier Rottenberg (Xavier.rottenberg@imec.be).

Software development and signal processing for high throughput silicon multi-electrode array systems

Cardiotoxicity is the major cause of drug withdrawal from the market, despite rigorous toxicity testing during the drug development process. This puts an enormous risk and pressure on pharmaceutical companies. Existing safety screening techniques (optical, impedance, cellular assays) are either too limited in throughput or offer too poor predictability of toxicity to be applied on large numbers of compounds in the early stage of drug development.
At imec, a new silicon multi-electrode array chip platform is developed that will address those challenges. This chip needs to be steered through a system that allows for amongst other features: electrode selection, uploading stimulation and recording parameters, controlling fluidic flow, customized user settings, etc. The intern project consists of the development of the graphical user interface for addressing chip functionality, high data rate transfer, (biological) data visualization, driver and USB communication, trouble shooting, multi-threading programming, etc. Advanced automated signal processing for in vitro cardiac signals and sorting will also be needed. We are looking for strong candidates with excellent knowledge of Visual studio C#, .Net, Matlab or Python. Understanding of VHDL and FPGA programming is a plus, as well as experience with biological signal processing.

Type of project: Internship project

Degree: Master in Science and Master in Engineering majoring in electrotechnics/electrical engineering, computer science

Responsible scientist(s):
For further information or for application, please contact Veerle Reumers (veerle.reumers@imec.be) and Dries Braeken (dries.braeken@imec.be).

V. Wireless Communication

Simulation and performance analysis of OFDM-MIMO radar

Thanks to the constant evolution of semiconductor technology, millimeter wave radars can now be implemented in a single chip including the transmitter, receiver and DSP. This highly integrated implementation makes consumer grade radar applications possible such as automotive radar, indoor or outdoor surveillance, gesture recognition and vital sign monitoring. Many radar waveforms are used in the radar community to accommodate various requirements such as resolution, ambiguity, maximum detection range, transmitted energy, complexity, etc... Typical waveforms are pulsed, stepped-frequency, stretch, PMCW and FMCW.
The use of an OFDM waveform in radar applications has recently emerged in the radar literature. The waveform present certain advantages such as precise spectrum engineering, digital communications capability and randomization/rejection of interference capabilities. It also has some disadvantages such as higher complexity, higher peak-to-average power ratio and possibly sensitivity to Doppler shifts.
In its radar program, imec has developed a complete simulation environment that simulates the transmitter, the propagation, the targets and the receiver. This simulator is very flexible and supports phased arrays, MIMO configuration, analog and RF non-idealities.
The goal of this thesis is to adapt the IMEC radar simulator to support the OFDM waveform, including for MIMO configurations. Other waveforms will also be considered if they are promising and if time allows.
The work will include:

- a literature survey
- implementation of OFDM (and possibly other waveforms) and OFDM-MIMO transmitter and receiver in the existing simulator
- evaluation of performances
- study of the impact of non-idealities
- investigation of innovative solutions

The successful candidate will have to show a strong understanding of radio transceivers and signal processing. Proficiency with Matlab is a must. Some knowledge of radar concepts is a plus.

Type of project: Thesis or thesis with internship project of 6 months

Degree: Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact André Bourdoux (andre.bourdoux@imec.be) and Ubaid Ahmad (ahmad.ubaid@imec.be).

60GHz communication prototyping on a fast FPGA platform

Communications at 60GHz is an emerging communication technology that has recently been standardized (IEEE802.11ad/WiGig) for fast market adoption. Future standards will probably emerge in a near future, with enhancements and more features. IMEC has developed such a 60GHz communications chip, integrating all the RF and analog hardware including beamforming capability.
The goal of this thesis is to implement transmitter and receiver signal processing algorithms on an advanced FPGA platform that will be interfaced with the imec 60GHz chip for performance evaluation and experimentation. The challenge resides in the very high speed of the signal processing, requiring careful architectural choices and parallelization. Additionally, the system requires high-speed connectivity to a PC combined with a software application that performs data post-processing and provides graphical output.

The applicant must have a sound understanding of digital signal processing. He/she must have a good background in digital circuit design (VHDL) and also have some experience with Matlab. Knowledge of digital communications principles, software development (C/C++) and Linux OS is a plus.

Type of project: Thesis project of 6 months

Degree: Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact André Bourdoux (andre.bourdoux@imec.be) and Meng Li (meng.li@imec.be).

Millimeter-wave radar experimentation

Thanks to the constant evolution of semiconductor technology, millimeter-wave radars can now be implemented in a single chip including the transmitter, receiver and DSP. This highly integrated implementation makes consumer grade radar applications possible such as automotive radar, indoor or outdoor surveillance, gesture recognition and vital sign monitoring. Many radar waveforms are used in the radar community to accommodate various requirements such as resolution, ambiguity, maximum detection range, transmitted energy, complexity, etc...
Imec has developed a high resolution CMOS radar chip including the millimeter-wave part, the ADC and the digital front-end. This chip is connected to a digital platform for further processing.
The goal of this thesis is to experiment with the imec radar (and possibly other radars) in various environments and for different applications. Large data sets must be collected and further analyzed to recognize application-dependent target features. Classifying those features will help in providing information beyond the classical range/speed/angle of the radar.
This work will be performed with a team working on all aspects of the radar, from RF to software.
The successful candidate will have to show a good understanding of radio transceivers and signal processing. Proficiency with Matlab and C/C++ is a must. Some knowledge of radar concepts is a plus.

Type of project: Thesis or thesis with internship project of 6 months

Degree: Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact André Bourdoux (andre.bourdoux@imec.be) and Ubaid Ahmad (ahmad.ubaid@imec.be).

VI. Image Sensors and Vision Systems

Data analysis of semiconductor production data

The CMORET department focusses on developing technology in various business lines like image sensors, mems and life science applications. This development process generates large amounts of data of various sources. Sources like production data collected during the semiconductor manufacturing process, logistic data, in process metrology as well as functional test data are all stored in a central SAS data warehouse. From this data valuable information can be extracted to ensure quality and on-time delivery of our products.
During this internship you will develop new and improve existing scripts to support the activity of data analysis on production data.
The ideal candidate loves to code, has experience with the SAS platform and is proficient in English.
Required skill sets: basic coding experience in SAS base and SAS macro code.
Optional : Experience with Python coding is a plus.

Type of project: Internship project

Degree: Master in Industrial Sciences and Master in Science and Master in Engineering majoring in physics, chemistry/chemical engineering, materials engineering, bioscience engineering, mechanical engineering, electrotechnics/electrical engineering, energy, computer science, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Gregor Vercaigne (gregor.vercaigne@imec.be).

Analysis of high dimensional data using machine learning and statistical approaches

The goal of this project is to analyze high dimensional data for characterizing and identifying certain biological entities. The data is acquired using hyperspectral imaging camera which results in a high resolution data, both spatially and spectrally.
The data analysis will require implementing and evaluating different approaches for –

- Data pre-processing
- Feature extraction and selection
- Classification and regression

Profile requirements:

- Extensive hands-on programming experience (Matlab, R or Python)
- Experience and knowledge in machine learning and statistical approaches

Added advantage

- Experience in image processing, multi/hyper-spectral imaging
- Experience with data analysis tools like WEKA

This is a venture development project and we are currently in the proof-of-concept stage. We expect to spin-out in next 6-8 months. There will be opportunity to join the startup team for data analysis and software development based on the performance during this internship.

Type of project: Internship project of 3 to 6 months based on availability (starting immediately)

Degree: Master in Science or Master in Engineering majoring in bioscience engineering, electrotechnics/electrical engineering, computer science

Responsible scientist(s):
For further information or for application, please contact Prashant Agrawal (prashant.agrawal@imec.be).

VII. Large Area Flexible Electronics

Infrared photodetectors using colloidal quantum dots

Most modern infrared photodiode arrays combine a silicon based backplane with an infrared absorbing material. These thick substrates are flip-bonded to the backplanes, which limits the pixel resolution. Processing directly on top of a silicone backplane will increase the pixel density and decreases the production cost. At the same time, this solution would open options to fabricate flexible photodetectors, processing the infrared materials on sheets in combination with flexible electronics.
In the recent years, colloidal quantum dots received an increasing amount of attention due to their opto-electronic properties, with applications in light-emitting diodes and photovoltaics. Once the size of a nanoparticle reaches the exciton Bohr radius, quantum confinement effects will affect both the light absorption and emission spectrum of the material. By starting from a bulk material with infrared absorbing properties, one can obtain visible or infrared absorbing quantum dots. The quantum dots are typically surrounded by organic ligands that stabilize the material. The material can be made soluble by selecting the correct ligand. Moreover, these ligands can limit the large surface recombination inherent to the small quantum dots.
The focus of this internship will be optimization of the fabrication process of advanced colloidal quantum dot based photodetectors and investigation of their performance with respect to industrial specifications. Active layers will be deposited by solution processed techniques such as spin-coating or blade-casting. The student will be involved in the entire fabrication cycle, performed in the state-of-the-art facilities including imec's cleanroom and dedicated thin-film line. Initially, the student will receive training on the relevant processing and characterization tools. After a short introduction to the facilities, an independent investigation is expected with the focus on short-term research goals. Internship of at least 6 months is required.

Type of project: Thesis or internship project or combination of both

Degree: Master in Industrial Sciences and Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering, electrotechnics/electrical engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Pawel Malinowski Pawel.Malinowski@imec.be) and David Cheyns (David.cheyns@imec.be).

Creating ultrasound on foil

Traditional microphone units focus on human perceptible sound waves (between 20 Hz and 20 kHz). Acoustic development also focuses on ultrasound, compromising the frequencies above the detection limit of the human ear (from 20 kHz to several GHz). These sound waves can be used for a wide variety of applications, including medical imaging, therapeutic treatment, non-destructive testing and position localization of objects. Nowadays, ultrasonic transducer and sensor technology is largely based on rigid bulk piezoelectric ceramic materials, such as lead zirconate titanate or barium titanate. Although a mature technology for discrete passive components, offering a reasonably wide bandwidth and sensitivity, this ceramic-based technology is not amenable to machine large two-dimensional (2D) transducer arrays. Also, monolithical integration with other electronic components such as signal processing electronics is hardly possible. This is crucial for applications where large arrays are needed and for which a high level of integration is clearly a must. In the past years, imec has led the development of novel technologies that promise to meet all requirements of future micro-sound systems. The Large Area Electronics (LAE) and System in Foil (SiF) technology platforms allow to produce passive and active components in thin-film frameworks with world-leading performance and in flexible form factors. Further, preliminary demonstrations of ultrasound components monolithically integrated with their drive and readout electronics are emerging. These developments support the perspective to develop multimodal ultrasonic sensing and acting skins. The purpose of this internship is to develop novel process flows for the next generation ultrasound transducers on large area technology. Depending on the

interest of the student, this can be coupled with mechanical and acoustic simulations to model the frequency and acoustic out-coupling of the devices.

Type of project: Thesis or internship project or combination of both

Degree: Master in Industrial Sciences and Master in Science and Master in Engineering majoring in physics, materials engineering, mechanical engineering, electrotechnics/electrical engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact David Cheyns (David.cheyns@imec.be).

Growth of highly ordered organic semiconductors

P-type thin film transistors (TFT) based on latest generation organic semiconductors (C8-BTBT, C10-DNTT) display excellent characteristics, with charge transport mobility of up to 10 cm2/Vs. These materials reach the quality levels of n-type oxide semiconductors (IGZO), potentially enabling the development of a complementary technology (CMOS) for low-cost electronic circuits on large area flexible foils. Examples of potential applications for such circuits are RFID tags, smart packaging, flexible displays and numerous biomedical applications.
Among other things, the performance of organic TFT depends on the degree of crystallinity of the organic semiconductors. Higher ordering delivers better performance, and, the best TFTs are based on defect free single organic crystals. The production of thin films of defect free organic single crystals over large area is therefore highly desirable. This, however, remains a considerable challenge since the presence of only a few defects will negatively impact the spread of TFT characteristics. As the spread increases, the yield of circuits dramatically decreases.
In this internship we propose to work on the development of techniques to achieve the growth of highly ordered organic semiconductor, following two routes. A first route is the development of substrate treatments that help to template the growth of organic-semiconductors and increase their degree of order. Templating, that relies on a good match between the crystal structures of the substrate and the grown material, is very well known in the field of epitaxial growth of inorganic materials. In the field of organic, however, much remains to be done. A second route is the optimization of the semiconductor growth technique, either from solution or from vapor. Achieving a high degree of order requires a spatial separation of the crystal nucleation event and the subsequent crystal growth. This is best achieved in a system involving linear motion that pulls a growing front.
The work is mainly experimental and will include substrate preparation and treatment, organic semiconductor deposition, either from the vapor phase or from a solution, and the fabrication of TFTs to characterize the electrical properties of the templated layers.

Objectives
For imec
- Explore the potential of substrate treatments to template the growth of high performance organic semi-conductors and achieve a better ordering.
- Optimize our highly ordered organic semiconductor fabrication technologies.

For the candidate
- Learn fabrication techniques that are relevant in microelectronics.
- Learn basics of crystal growth and TFT characterization.
- Learn the design of experiments.
- Work as a team in a professional research environment.

Skills required
- Material science background
- Knowledge in electronics
- Handy in the lab
- Self-motivated and independent hard worker

Type of project: Thesis with internship project

Degree: Master in Science and Master in Engineering majoring in physics, materials engineering, electrotechnics/electrical engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Cédric Rolin (Cedric.Rolin@imec.be).

Organic patterning

The ever-increasing resolution of displays and imagers fabricated using organic semiconductors requires new, advanced patterning techniques. Currently, the most popular fabrication process for high-resolution displays based on thermally-evaporated OLED stacks is shadow-masking. Still, this technology has limitations in terms of the smallest feature size and up-scalability for very large substrate sizes. As an alternative, dedicated photolithography processes can be used. In this case, special care needs to be taken to ensure chemical compatibility of the processing products used with the very fragile organic compounds. Imec is active in developing novel solutions enabling patterning of advanced organic semiconductor devices by photolithography. The focus of this internship will be optimization of the fabrication process of high-resolution organic photodetectors and light emitting diodes. Active layers will be deposited by spin-coating (solution processed polymers) or thermal evaporation (evaporated small molecules). The student will be involved in the entire fabrication cycle, performed in the state-of-the-art facilities including imec's cleanroom and dedicated organic line. Initially, the student will receive training on the relevant processing and characterization tools. After a short introduction to the facilities, an independent investigation is expected with the focus on short-term research goals. As this internship is focused on the photolithography aspects of the semiconductor fabrication route, experience in this domain is a necessity.

Type of project: Internship project (minimum duration of 6 months)

Degree: Master in Industrial Sciences and Master in Science and Master in Engineering majoring in physics, materials engineering, electrotechnics/electrical engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Pawel Malinowski (Pawel.Malinowski@imec.be) and TungHuei Ke (Tung.Huei.Ke@imec.be).

To investigate different source-drain metal integration in a-IGZO TFT structures

Amorphous oxide semiconductors (AOSs) are of great interest for thin-film transistor (TFT) channel layer applications. They have been studied due to their superior characteristics, such as high uniformity, high electron mobility (10-50 cm2/V·s), and their fabrication at low temperatures on plastic substrates. These advantages of a-IGZO TFTs are promising for next-generation backplanes for displays and circuits on the transparent and flexible substrate.
Currently in our self-aligned (SA) TFTs, the S/D metal is integrated with few limitations on the minimum metal line dimensions (feature size and thickness) and resistivity. For the future large area applications, the S/D metal line dimensions and resistance (contact and line) need to be reduced. The objective of this internship is to integrate different low resistive S/D metals using etch process in the SA and dual-gate TFTs. The student investigates both wet and dry (fluorine and chlorine based chemistry) etch methods. The integration also includes the change in the intermetal layer if required. Excellent TFT characteristics of the final TFT stack on the flexible substrate are expected. From the results a conclusion need to be drawn on the integration issues and material of the S/D metal layer. This activity also includes the measurements of the fabricated devices.

Type of project: Internship project

Degree: Master in Industrial Sciences and Master in Science and Master in Engineering majoring in physics, materials engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Manoj Nag (Manoj.Nag@imec.be) and Kris Myny (Kris.Myny@imec.be).

VIII. Solar Cells and Batteries

Development and characterization of high band-gap thin films for use in solar cells

Today, record single-junction solar cell efficiencies are approaching their theoretical limit of 30 % under 1-sun illumination. One method to increase efficiency even further is the development of tandem solar cells. A tandem solar cell consists of two cells: a high band-gap cell (1.5-2.0 eV) harvests the high-energy photons and a lower band-gap cell (1.0-1.5 eV) harvests the low-energy photons. This approach leads to theoretical efficiencies of 44 % under 1-sun illumination. However, tandem solar cell development has been mainly focused on costly materials; and is not yet feasible at low-cost as there is no stable and abundant high band-gap top cell alternative demonstrated. See [1,2]. For that reason the thin film (TF) solar cell group in Imec studies novel high band-gap TF materials with potential to be low-cost. Within this group, TF materials based on the Cu2ZnSn(S,Se)4 (CZTSSe) material system are developed and characterized, but also tested in actual solar cells. The aim is to enhance the scientific understanding of these materials and to develop novel solar cell technologies. This study started in 2011 with the development of pure selenide sputtered CZTSe thin films; wherefore a state-of-the-art top efficiency of 10.4 % has been obtained. More recently, also CZTGeSSe (and CTZSiSSe) TF materials are developed and studied; early research indicating that substitution of Sn with Ge (resp. Si) in the CZTSSe crystal lattice leads to an increase in band-gap and enhanced material quality. See [3,4].
This study of similar and other interesting high band-gap TF candidates remains at the forefront of TF solar cell research, where physicists, engineers and chemists have the ability to successfully contribute. So, if you are interested in this work, then please contact the supervising scientist to find out if your profile fits this research.

[1] M.A. Green, K. Emery, Y. Hishikawa, W. Warta, E.D. Dunlop, Progress in Photovoltaics: Research and Applications 24(1):3-11, 2016.
[2] T.P. White, N.N. Lal, K.R. Catchpole, IEEE Journal of Photovoltaics 4(1):208-214, 2014.
[3] M. Buffière, H. ElAnzeery, S. Oueslati, K. Ben Messaoud, G. Brammertz, M. Meuris, J. Poortmans, Thin Solid Films 582:171-175, 2015.
[4] S. Oueslati, G. Brammertz, M. Buffière, H. ElAnzeery, O. Touayar, C. Köble, J. Bekaert, M. Meuris, J. Poortmans, Thin Solid Films 582:224-228, 2015.

Type of project: Thesis or internship project or combination of both

Degree: Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering, electrotechnics/electrical engineering, energy, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Bart Vermang (bart.vermang@imec.be).

Optimization of the performance of CZTSe solar cells

In addition to our study of novel high band-gap CZTGeSSe and CTZSiSSe thin film (TF) materials, see [1], we are still optimizing our pure-selenide CZTSSe solar cell baseline. At present, the standard CZTSSe solar cell structure is grown on a (soda lime) glass substrate. Its growth process starts with an optional diffusion barrier layer (to avoid in-diffusion of unwanted elements from the substrate), followed by a molybdenum (Mo) rear-contact, a CZTSSe absorber layer and a CdS or Cd-free buffer layer, and finishes with a transparent conductive oxide layer (typically i-ZnO/ZnO:Al) as front-contact. See Figure 1 for a cross-section of such a standard CZTSSe solar cell fabricated at Imec. The world record CZTSSe solar cell efficiency is 12.6 %.

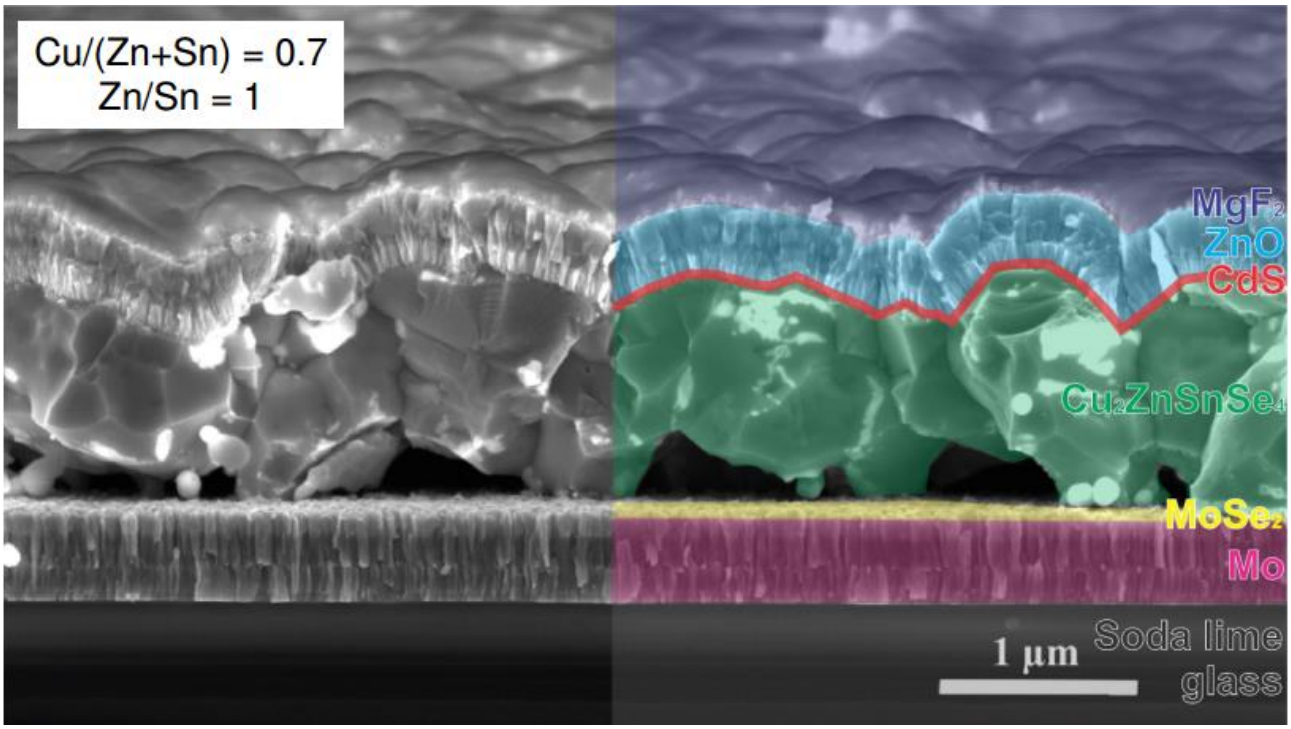


Figure 1: Cross section secondary electron emission picture of a pure selenide CZTSe solar cell fabricated at Imec, with a 10.4 % record efficiency. Note that a MgF2 anti reflection coating has been applied.

At imec, we are constantly optimizing this CZTSSe solar cell fabrication process. A very interesting optimization study for physicists, engineers and/or chemists, as it gives them the opportunity to acquire essential understanding of solar cell development and characterization. If you are interested in this work, then please contact the supervising scientist to find out if your profile fits this research.

[1] MS project topic "Development and characterization of high band-gap thin films for use in solar cells".

Type of project: Thesis or internship project or combination of both

Degree: Master in Science and Master in Engineering majoring in physics, chemistry, materials engineering, electrotechnics/electrical engineering, energy, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Bart Vermang (bart.vermang@imec.be).

Measurement and demonstrators for innovative smart PV modules under non-uniform irradiation

It is well known that photovoltaic (PV) modules yield a lower energy in the field than what could be expected from their rated power, indicated as "peak-Watts (Wp)". This rating is determined, according to an industrially and internationally accepted standard, under "Standard Test Conditions (STC)". These conditions involve amongst others an irradiance of 1000 W/m2 ("AM1.5 spectrum"). Knowing that these values, in climates such as Belgium's, can only be maintained for longer periods of time on very sunny days with clear skies, it is clear that these conditions are relatively rare throughout the year and indeed the rated power effectively only indicates "peak" performance of the module.
In fact, the main energy yield losses (kWh/kWp), in particular in Belgium, can be attributed to a reduced illumination resulting in lower current and non-uniform illumination conditions (shading, clouds, soiling, ...) leading to current mismatch in the serially connected cells inside the module.
Therefore, in this topic, we want to measure the impact of such non-uniform and dynamic irradiation and shading conditions using an illumination setup for large-area (1x1.6m2) PV modules in order to more accurately evaluate panels in conditions that are closer to reality. Concretely, we want to be able to illuminate at lower irradiance levels, that can be applied with spatial non-uniformity and that can be varied in time. Apart from testing and characterizing the PV modules and (partly also) the setup itself, we want to use it to assess the performance of advanced "smart|" PV modules we are building|. They have configurable non-series topologies for which we want to evaluate the Eyield under many different shading conditions. We also want to finalize more of such configurable module demonstrators with specific topologies.
Measurements with this illumination setup and the demonstrator modules will then later on (outside the scope of this topic) be used to validate some complex optical-thermal-electrical models we are building to predict and evaluate the potential energy gain of future smart PV modules (WHAT-IF analysis).
The entire project will have a clear impact on relevant aspects of the future photo-voltaic energy landscape. It combines mostly practical skills with a more in-depth analysis of the obtained results. Considering the variety in challenges to be addressed within this topic (electronic hardware, control software, PV characterization, interpretation and extrapolation), it is important for us to have a candidate who already has a broad background in this domain. However, given that we work on this with a team, the specific focus of the MSc subgoals within the topic can be adapted to some extent to the interest of the applicant.

Type of project: Thesis project
This project is only open to self-supporting students (no imec allowance will be provided). The start date of the project is Q2/Q3, 2017.

Degree: Master in Engineering majoring in electrotechnics/electrical engineering, energy

Responsible scientist(s):
For further information or for application, please contact Jonathan Govaerts (Jonathan.govaerts@imec.be) and Francky Catthoor (Francky.Catthoor@imec.be).

Modeling and measurement analysis of energy yield for advanced and smart PV modules

Photovoltaic (PV) solar panels provide a very attractive solution for future clean energy provision on-site. State-of-the-art, optimally installed PV modules preform excellent during clear-sky conditions. However, their energy yield reduces dramatically during non-steady state and installed at places which suffer from non-uniform illumination (e.g. static shading created by tree).
Imec is developing PV modules with additional or novel components to improve energy yield, especially during high-varying conditions and non-uniform illumination . First prove-of-concept modules are being installed and monitored to investigate the energy yield of these advanced and smart configurable PV modules. The electrical characteristics

of PV modules depend on ambient conditions like ambient temperature, irradiance, wind speed and wind direction. Due to the highly varying character of these parameters, high frequency measurements are required in order to evaluate energy yield of the smart PV modules. Furthermore, more and more conventional PV systems are monitored nowadays. Both measurement campaigns creates an enormous stream of valuable information. In order to prove the benefits of additional components, or to detect faulty PV systems, we need to analyze this information.
The student will have to collect, combine and analyze information coming from both smart PV modules, as well as information from conventional PV systems. The student has to use this analysis to identify potential gains under each specific situation. If required, the student can perform additional (indoor or outdoor) measurements. Furthermore, the student will analyze energy yield of advanced and smart PV modules to improve existing electrical-thermal Eyield models. Also WHAT-IF explorations will be tried out with the resulting models.
The entire project will have a clear impact on relevant aspects of the future photo-voltaic energy landscape. It combines mostly practical skills with a more in-depth analysis of the obtained results. Considering the variety in challenges to be addressed within this topic (electronic hardware measurement, control software, PV characterization, modeling), it is important for us to have a candidate who already has a broad background in this domain. However, given that we work on this with a team, the specific focus of the MSc subgoals within the topic can be adapted to some extent to the interest of the applicant.

Type of project: Thesis or thesis with internship project
This project is only open to self-supporting students (no imec allowance will be provided). The start date of the project is Q2/Q3, 2017

Degree: Master in Industrial Sciences and Master in Engineering majoring in electrotechnics/electrical engineering, energy

Responsible scientist(s):
For further information or for application, please contact Jonathan Govaerts (Jonathan.govaerts@imec.be), Francky Catthoor (Francky.Catthoor@imec.be) and Hans Goverde (Hans.goverde@imec.be).

Next generation PV module technologies

Photovoltaics panels around us are mainly (over 80%) based on c-Si solar cells, and this will continue to be the case for the foreseeable future. The module technology used for connecting and protecting these cells likewise has been established already long time ago. The currently standard module technology is based on stringing of cells for electrical interconnection and subsequent EVA lamination for encapsulation of these strings between a (transparent) front- and backsheet. This technology has proven its worth with operational lifetimes exceeding 20 years in harsh outdoor conditions. However it is time for change! Untapped potential of advanced materials and novel low-stress interconnection technologies integration in PV modules can bring a new era of innovation in traditional PV module fabrication. With this in mind, with its extensive expertise in cell technology, imec is starting to develop advanced module concepts. Several internship topics are proposed on the following subjects:

- Low-stress interconnection technologies are indispensable for the integration of thinner and more advanced cells in PV modules. We are investigating at imec unique concept suited both for traditional, bifacial and back contact solar cells using low temperature solder alloys. One of the first technical challenges is the selection of materials for reliable solder joints, their process integration and electrical and material testing with adhesion and interdiffusion studies..
- Simulation of the optical potential of novel materials in module design: First relying on an open-access simulation tool the advantage of new materials should be quantified. Both to provide input and validate the modelling dedicated samples, small laminates will be prepared and characterized. Limitation of the existing simulation tools might be overcome by defining own simulation framework.
- Reliability investigation of novel encapsulation materials in combination of traditional and novel cell types. Relevance of currently used accelerated reliability tests should be validated by first monitoring the performance loss of samples under different stress conditions and comparing with samples exposed to operational conditions. In parallel the impact of novel stress conditions and/or sequence of stress tests will be explored. Finally, understanding the root-cause of the failure in the different conditions will be critical part of the investigation.

These topics are multi-disciplinary in nature, as they look both at the technology for PV module fabrication (with limited size), as well as the materials and opto-electrical characterization and operation aspects of those modules. The focus can be adapted to some extent to the interest and capabilities of the applicant. Most of the work will be done in the state-of-the-art device processing lab of IMEC. The student will receive a broad training on full device processing and characterization tools. After a short training period it is expected that the student can work independently and focusing on his/her investigation.

Type of project: Internship project
This project is only open to self-supporting students (no imec allowance will be provided).

Degree: Master in Industrial Sciences and Master in Science and Master in Engineering majoring in electrotechnics/electrical engineering, energy, physics, materials engineering

Responsible scientist(s):
For further information or for application, please contact Jonathan Govaerts (Jonathan.govaerts@imec.be), Tom Borgers (Tom.borgers@imec.be) and Eszter Voroshazi (Eszter.voroshazi@imec.be).

Optoelectronic characterization of high band gap thin film solar cells

Next to Si-based solar cells, devices based on chalcogenide thin films, such as CdTe and Cu(In,Ga)(S,Se)2 (CIGS), are at the forefront in thin film solar cell technology. However, reliance on the heavy metal Cd and on the non-abundant elements In and Te presents a major barrier towards meeting the multi-terawatt-scale target for renewable energy supplied by photovoltaics. Moreover, thin film PV has to compete with present efficiencies of silicon solar cells above 20%. Therefore, multi-junction PV solutions will be needed in the future.
Chalcogenide materials such as Cu2Zn(Sn,Ge)(S,Se)4 and Cu2Si(S,Se)3 are emerging alternative solar cell absorbers that provide diversification away from the non-earth-abundant elements mentioned above and have the promise of the development of a multi-junction thin film solar cell. Depending on the exact stoichiometry and choice of the different elements in the absorber, the band gap of the absorber can be varied between 1 and 2 eV, which makes the combination of different absorbers into multi-junction thin film solar cells or multi-junction thin film-Si solar cells possible.
This master thesis topic consists of electrical and optical characterization of these novel absorber layers and solar cells.
Electrical measurements to be performed consist of current-voltage and capacitance-voltage measurements of thin film solar cell structures. All measurements will be performed as a function of temperature and illumination intensity, in order to fully characterize the diode parameters of the solar cell structure and to gain insight into the dominant recombination processes in the cell.
Optical measurements to be performed consist of temperature and intensity dependent photoluminescence and time-resolved photoluminescence measurements. These measurements will allow further insight into the different recombination mechanisms in the solar cells.
The different characterizations will be linked to the growth of the absorber in order to optimize the absorber quality for solar cell applications.

Type of project: Thesis project

Degree: Master in Science and Master in Engineering majoring in physics, materials engineering, electrotechnics/electrical engineering, energy, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Guy Brammertz (brammert@imec.be).

Solid composite electrolyte for lithium ion batteries

Lithium ion batteries (LIB) capture about 70% of the portable electronics market and will gradually replace the nickel-metal hydride batteries in hybrid electrical vehicles (HEV). The energy and power density of existing battery technology is however not sufficient . Therefore, innovations in battery technology are badly needed and the inclination for disruptive technologies grows. Solid electrolytes are being explored to replace the flammable liquid electrolyte currently used in both inorganic and polymer Li-ion batteries. Next to resolving the issues with safety, which is imperative for automotive applications, the transition to a solid-state electrolyte would mean significant improvements in the battery performance as well: higher energy density, longer battery life time and wider temperature range of operation. Solid composite electrolytes are promising candidates. In composite electrolytes, higher Li-ion conductivities are obtained at the interface between a Lithium salt and an inert material such as alumina and silica. In our lab, we have fabricated composite electrolyte with high conductivity via sol-gel method. The properties of the electrolyte could be improved further. Compatibility of the electrolyte with the electrode is to be explored. You will seek and understanding of the chemistry and optimize the sol-gel process to improve the conductivity of the electrolyte. The interface interaction in the solid composite electrolyte is to be investigated. You can learn useful electrochemical techniques (eg. cyclic voltammetry, electrochemical impedance spectroscopy) from experts. For compositional and structural characterization, you will be introduced to analysis techniques such as FTIR, DSC, XRD, SEM, TEM, XPS, TOFSIMS etc.

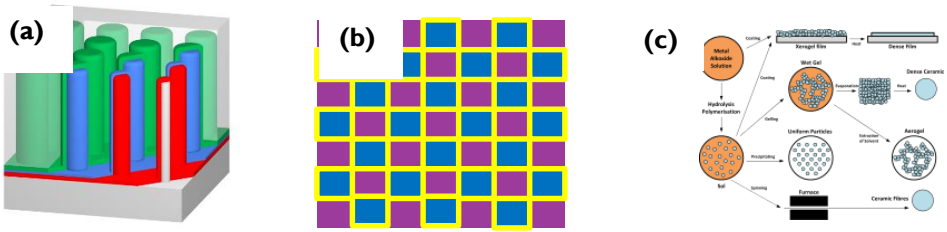


Figure 1: Schematic diagram of (a) all-solid state battery , (b) composite electrolyte (c) Sol-gel process

Type of project: Thesis or thesis with internship project

Degree: Master in Science and Master in Engineering majoring in chemistry/chemical engineering, materials engineering, bioscience engineering, nanoscience & nanotechnology, energy

Responsible scientist(s):
For further information or for application, please contact Philippe Vereecken (Philippe.Vereecken@imec.be) and Xubin Chen (chenxu@imec.be).

Enhancing stability in thin film solid state batteries

In the past decade lithium-ion batteries (LIB) have gained much attention in portable consumer electronics due to their high-energy density, high voltage, excellent shelf life and safety, which makes them the best choice for rechargeable batteries for devices such as mobile phones, laptop computers, tablets and energy harvesters. Although LIBs have already captured most of the portable electronic market there are still significant improvements that have to be investigated in order to improve the current state-of-the art technology. Although solid electrolytes seem to be promising in LIBs they still have poor ionic conductivity at acceptable working temperatures. Novel materials and interfacial buffer layers have to be explored in order to overcome this obstacle and increase ionic conductivity and stability in electrode-compatible electrolytes. Recently a novel type of glass has reported the highest ionic conductivity for Li-ions. Glassy electrolytes are a fairly recent type of materials that are being explored in the world of Li-ion batteries. Achieving the highest ionic conductivity and manipulating it by optimizing electrolyte deposition

conditions and enhancing stability by using intercalating buffer layers may be a breakthrough in thin film solid-state batteries in the near future. The challenge of this project is the creation, test and operation of different structures while still maintaining a proper mechanical integrity to increase overall lifetime performance.
Thin film deposition can be done in several high-tech equipment available in IMEC (i.e. sputtering, ALD). A number of tools are available for material characterization to investigate morphology and structure, electrical performance and electrochemical behavior (i.e. SEM, impedance spectroscopy, galvanostatic/potentiostatic). The main objectives of this work will be to: 1) study the intercalation effect of different layers between an electrode/electrolyte interface using half cell stacks. (i.e. material) 2) Identify buffer layer conditions for optimum capacity and rate performance. (i.e. thickness) 3) Study electrolyte deposition conditions in order to increase ionic conductivity and electrode/electrolyte interface. (i.e. depotision temperature) 4) Create an all-solid thin film stack using buffer layer interfaces. The student involved in this project will acquire expertise in nano-materials through applying different deposition methods for film growth and using several material characterization tools. He/she will improve his/her knowledge in physical chemistry, electrochemistry, material science and thin film technology.

Type of project: Thesis project

Degree: Master in Science and Master in Engineering majoring in physics, chemistry/chemical engineering, materials engineering, materials engineering, bioscience engineering, nanoscience & nanotechnology, energy

Responsible scientist(s):
For further information or for application, please contact Alfonso Sepúlveda Márquez (alfonso.sepulvedamarquez@imec.be).

Design and evaluation of local DC-DC convertor circuit topologies for smart configurable PV modules

It is well known that photovoltaic (PV) modules yield a lower energy in the field than what could be expected from their rated power, indicated as "peak-Watts (Wp)". This rating is determined, according to an industrially and internationally accepted standard, under "Standard Test Conditions (STC)". These conditions involve amongst others an irradiance of 1000 W/m2 ("AM1.5 spectrum"). Knowing that these values, in climates such as Belgium's, can only be maintained for longer periods of time on very sunny days with clear skies, it is clear that these conditions are relatively rare throughout the year and indeed the rated power effectively only indicates "peak" performance of the module. In fact, the main energy yield losses (kWh/kWp), in particular in Belgium, can be attributed to a reduced illumination resulting in lower current and non-uniform illumination conditions (shading, clouds, soiling, ...) leading to current mismatch in the serially connected cells inside the module.
In order to maximize the power production of PV modules working under non-uniform illumination conditions, we are building advanced "smart" PV modules able to dynamically establish different non-series topologies. For them, we want to evaluate the Energy yield under many different shading conditions. We also want to finalize more of such configurable module demonstrators with specific topologies, and to validate them by experimentally evaluating the Energy yield gain they allow for when working under non-uniform and dynamic irradiation and shading conditions, with respect to standard state-of-the-art serially connected topologies.
Currently, we are mainly interested in designing and prototyping local DC/DC converters to finalize the first smart PV module demonstrator. These local convertors have quite different specs from more conventional string or even module level convertors because they aim at much lower voltage and current levels, and they do not require the overhead of a maximum power point tracker (MPPT).
The circuit design is still challenging though because voltages up to 10V input and 30V output, and current levels up to 30A have to be sustained. Moreover, the stability of the voltage(s) imposed by the (separate) control module should be ensured by tracking. For this purpose, thorough SPICE level circuit simulations are essential. Depending on the outcome of this circuit exploration also contributions to the smartPV hardware demonstrators will be added. The entire project will have a clear impact on relevant aspects of the future photo-voltaic energy landscape. It combines mostly practical skills with a more in-depth analysis of the obtained results. It will also be co-guided with colleagues from the Univ. of Ghent and part of the MSc activities will take place in their location. Considering the variety of challenges to be addressed while designing such converters, it is important for us to have a candidate who

already has a strong background in the domains of power electronics, preferably applied to photovoltaic sources, and control. However, given that we work on this with a team, the specific focus of the MSc subgoals within the topic can be adapted to some extent to the interest of the applicant.

Type of project: Thesis or internship project or combination of both
The start date of the project is Q2/Q3, 2017.

Degree: Master in Industrial Science and Master in Engineering majoring in energy, electronics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Patrizio Manganiello (Patrizio.Manganiello@imec.be), Francky Catthoor (catthoor@imec.be) and Pieter Bauwens (Pieter.Bauwens@elis.ugent.be).

Novel carrier selective contacts for new concept silicon solar cells

Photovoltaic(PV) energy is getting more attention since it is clean and sustainable energy source. However, the levelized cost of energy(LCOE €/W) of PV energy has to be reduced to compete with other energy sources for expanding PV markets. To follow up those needs, many technologies are under investigation for higher efficiency, more cost effective process and new concept silicon solar cells.
imec is the top leading research institute in PV research field including next generation of PV technologies. Furthermore, many talented imec researcher and a state of art facility facilitate more rapid technological progress. A student will work as a part of the excellence during the internship.

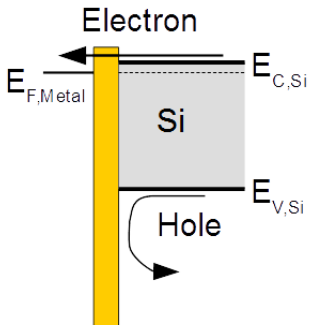


Figure 1. A Schematic concept of carrier selective contact. (A simple band diagram for electron contact.)

Internship student's research will focus on the contact of solar cells, especially on novel electron contacts which has low schottky barrier height and low carrier recombination at the contacts. The student will have to collect, combine and analyze information coming from materials, as well as structure of contacts. The student also has to use analysis methods to identify the back ground of the results of each specific cases. Quasi-Steady-State Photoconductance (QSSPC) lifetime measurement and J-V measurement will mainly be used to characterize the contact performance. At the end of the work, developed technologies will be integrated to the silicon solar cells.

Type of project: Internship project of 9 months - It is expected that the student presents his results in meetings, and writes high-quality reports at the conclusion of the internships (this can be a thesis).

This project is open to self-supporting students only (no imec allowance will be provided).

Degree: Master in Science and Master in Engineering majoring in material science, physics, electronics and any major related semiconductor technology

Responsible scientist(s):
For further information or for application, please contact Jinyoun Cho (jinyoun.cho@imec.be).

IX. Sensor Systems for Industrial Applications

On-chip photoacoustic spectrometry setup

Safety is a major concern these days. Quick and real time monitoring or trace detection of hazardous compound are key component on the field . Photoacoustic (PA) spectroscopy offers those points with a more compact setup than conventional IR ones.
A basic PA spectroscope setup is presented in the figure below (Figure 1). The laser beam(1) is chopped(2) in order to create an intensity modulation of the enlightening of the gas chamber(6,8) containing an analyte. This will absorb photons and, after a transition time, returns to its ground state by releasing vibrational and rotational energy. It will result in a localized heating and sudden raise of pressure. As the incident laser light is modulated in intensity, a pressure wave is generated with the same frequency. If the frequency of modulation corresponds to one of the resonance frequencies of the gas chamber, amplification of the generated sound occurs. A microphone(7) – strategically placed- picks the signal. By continuously tuning the laser wavelength, the analyte absorbs more or less photons regarding its absorption specter: the sound intensity will be modulated accordingly and the absorption specter is retrieved at the microphone.
The advantage of this spectroscopy technique lies mostly in the obtained specter: when the signal is drown in a huge background in conventional IR spectroscopy, PA have none: the signal is against zero background (Figure 2) . This confers to PA spectroscope the ability to detect and measure analyte concentration in the ppb (part per billion) region. The setup can be thus used as a spectrometer too.
Basic PA setups are typically bulky and efforts are made in order to miniaturize it. Therefore, the goal of this master thesis is to demonstrate miniature PAS system and study its scaling towards eventually fitting the whole setup (IR laser, tuning system, gas chamber and microphone) on a single chip. In order to achieve this, a better understanding of the phenomenon involved in PA and accurate simulation are needed to correctly predict the behavior of newly designed setups.
For this work we are therefore looking for enthusiastic students with strong simulations background and interest that should feel comfortable in the lab, building, assembling and using measurement setups.

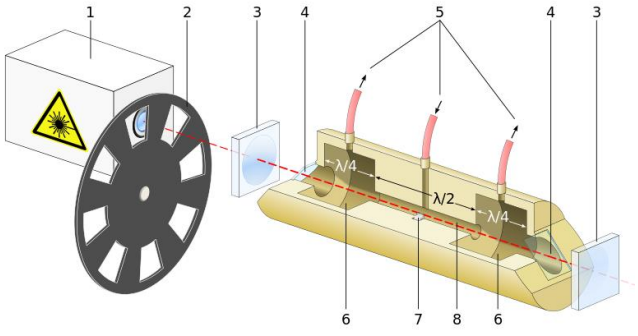


Figure 1. Basic photoacoustic spectroscope setup. Selective details are described in the text.

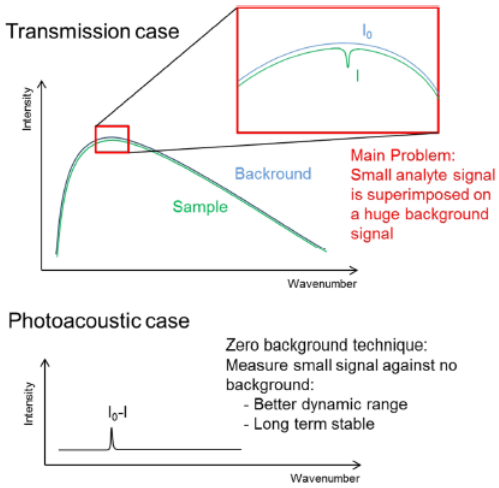


Figure 2. Graphical illustration of the indirect transmission and direct photoacoustic measurement.

Type of project: Thesis or internship project or combination of both

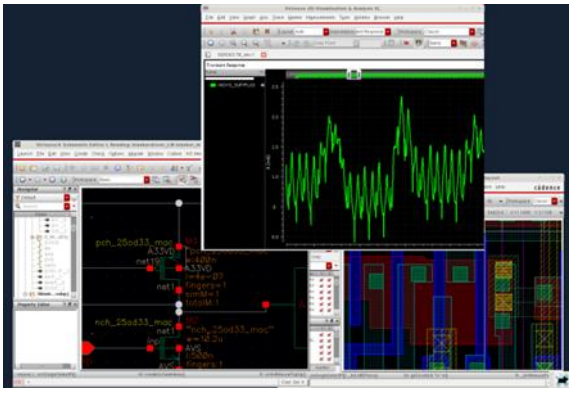
Degree: Master in Industrial Sciences and Master in Science and Master in Engineering majoring in physics, bioscience engineering, nanoscience & nanotechnology, computer science

Responsible scientist(s):
For further information or for application, please contact Rachid Haouari (Rachid.Haouari@imec.be), Xavier Rottenberg (Xavier.Rottenberg@imec.be) and Veronique Rochus (Veronique.Rochus@imec.be).

X. Microelectronic Design

Ontwerp van een spanningsreferentie in 65nm CMOS voor ruimtevaarttoepassingen

In deze thesis wordt de student vertrouwd gemaakt met 65nm CMOS ontwerp op transistorniveau. Het doel van het eindwerk is het ontwerp van een temperatuuronafhankelijke spanningsreferentie die bestand is tegen kosmische straling.
Imec IC-link ontwikkelt in samenwerking met het European Space Agency (ESA) al meer dan 10 jaren radiatie-tolerante digitale standaard-cel-bibliotheken en full-custom IP blokken in 180nm CMOS. Deze basisblokken worden gebruikt in IC's voor de ruimtevaartindustrie. Omdat hoog energetische straling de normale werking van elektronische schakelingen kan beïnvloeden en zelfs tot vernietiging ervan kan leiden, is er nood aan hoogwaardige radiatie-tolerante elektronica.
Om performantere radiatie-tolerante chips te kunnen ontwikkelen is de overstap naar 65nm CMOS DARE (Design Against Radiation Effects) essentieel. Met Imec IC-link willen we een oplossing aanreiken door het gamma aan DARE bouwblokken uit te breiden naar de 65nm CMOS procestechnologie.



Om on-chip een temperatuuronafhankelijke spanning te genereren wordt een "bandgap reference" (BGR) gebruikt. Deze thesis bestaat erin om dergelijke BGR stralingstolerant te ontwerpen in 65nm CMOS. De student vertrekt van een literatuurstudie die zich toespitst op stralingstolerant ontwerp enerzijds en het verkennen van verschillende BGR circuits anderzijds. Hierna volgt de ontwerpfase waarin een transistor-level schema wordt ontworpen en gesimuleerd. Na validatie van de specificaties (stabiliteit, nauwkeurigheid, stralingstolerantie,...) wordt overgaan naar de layoutfase: het schema wordt omgezet naar een 'mask design' waarmee de foundry de chip kan produceren in silicium.
Om de volledige specificatie-tot-layout flow te doorlopen, krijgt de student toegang tot state-of-the-art CAD software. Hiervoor is regelmatige aanwezigheid op imec vereist. De gebruikte software bestaat uit:

- Cadence Virtuoso (schema & layout), Analog Design Environment XL (simulatie)
- Mentor Calibre (layout verificatie)
- Linux OS

Tijdsindeling: 20% literatuurstudie, 50% ontwerp/simulatie, 30% layout

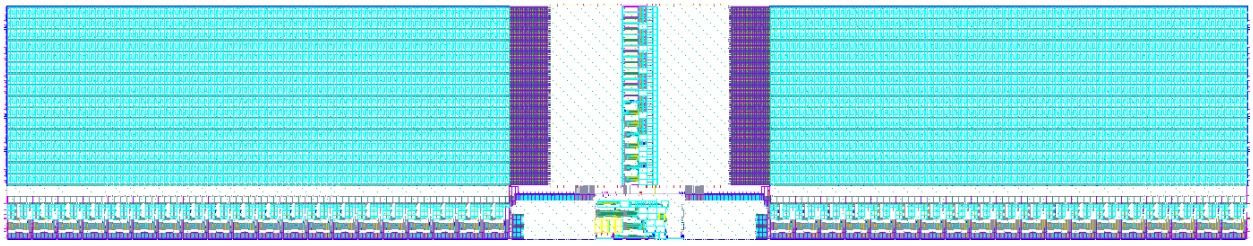
Type of project: Thesis with internship project

Degree: Master in Industrial Sciences majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Geert Thys (geert.thys@imec.be).

Ontwerp van een ROM-geheugens in 180nm CMOS voor ruimtevaarttoepassingen

In deze thesis wordt de student vertrouwd gemaakt met 180nm CMOS ontwerp op transistorniveau. Het doel van het eindwerk is het ontwerp van elektronische schakelingen voor een Read-Only-Memory (ROM) generator.
Imec IC-link ontwikkelt in samenwerking met het European Space Agency (ESA) al meer dan 10 jaren radiatie-tolerante digitale standaard-cel-bibliotheken en full-custom IP blokken in 180nm CMOS. Deze basisblokken worden gebruikt in IC's voor de ruimtevaartindustrie. Omdat hoog energetische straling de normale werking van elektronische schakelingen kan beïnvloeden en zelfs tot vernietiging ervan kan leiden, is er nood aan hoogwaardige radiatie-tolerante elektronica.
Frequent is er nood aan niet-vluchtige geheugens op zulke chips. Om niet telkens een geheugen van nul af te moeten opbouwen, worden geheugens gegeneerd via software die de specificaties (aantal woorden, woordbreedte, ..) automatisch vertalen in een combinatie van vooraf gemaakte en geverifieerde elementaire blokken.
Het doel van deze thesis is het uitwerken van alle basisblokken om de ROM-compiler 'correct-by-design' te laten functioneren. Dit houdt het ontwerpen van zowel schema's als layouts in.



Om de volledige specificatie-tot-layout flow te doorlopen krijgt de student toegang tot state-of-the-art CAD software. Hiervoor is regelmatige aanwezigheid op IMEC vereist. De gebruikte software bestaat uit:

- Cadence Virtuoso (schema &layout), Analog Design Environment XL (simulatie)
- Mentor Calibre (layout verificatie)
- Linux OS

Tijdsindeling: 15% literatuurstudie, 35% ontwerp/simulatie, 50% layout

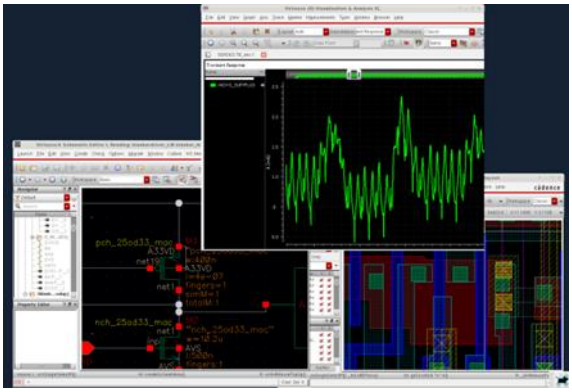
Type of project: Thesis with internship project

Degree: Master in Industrial Sciences majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Geert Thys (geert.thys@imec.be).

Evalueer en ontwerp register files of multi-bit registers in 65nm CMOS voor ruimtevaarttoepassingen

In deze thesis wordt de student vertrouwd gemaakt met 65nm CMOS ontwerp op transistorniveau. Het doel van het eindwerk is een oppervlakte-efficiënte oplossing voor kleine geheugens.
Imec IC-link ontwikkelt in samenwerking met het European Space Agency (ESA) al meer dan 10 jaren radiatie-tolerante digitale standaard-cel-bibliotheken en full-custom IP blokken in 180nm CMOS. Deze basisblokken worden gebruikt in IC's voor de ruimtevaartindustrie. Omdat hoog energetische straling de normale werking van elektronische schakelingen kan beïnvloeden en zelfs tot vernietiging ervan kan leiden, is er nood aan hoogwaardige radiatie-tolerante elektronica.
Om performantere radiatie-tolerante chips te kunnen ontwikkelen is de overstap naar 65nm CMOS DARE (Design Against Radiation Effects) essentieel. Met Imec IC-link willen we een oplossing aanreiken door het gamma aan DARE bouwblokken uit te breiden naar de 65nm CMOS procestechnologie.



Om geheugens en registers radiation tolerant te maken moeten bepaalde design technieken toegepast worden die grote area en power overhead hebben. Een deel van die overhead kan voorkomen worden voor kleine geheugens door slimme keuze van opties voor registerfiles of het gebruik van multi-bit registers. In het eerste stuk van het eindwerk wordt gekeken naar mogelijke oplossingen en een vergelijking gedaan van de voor- en nadelen van elk. In het tweede deel wordt dan een gekozen oplossing geïmplementeerd.
Om de volledige flow te doorlopen, krijgt de student toegang tot state-of-the-art CAD software. Hiervoor is regelmatige aanwezigheid op imec vereist. De gebruikte software bestaat uit:

- Synopsys Design Compiler (synthesis)
- Cadence Virtuoso (schema & layout), Analog Design Environment XL (simulatie)
- Mentor Calibre (layout verificatie)
- Linux OS

Tijdsindeling:

- 20% literatuurstudie
- 30% vergelijkende studie
- 30% ontwerp/simulatie
- 20% layout

Type of project: Thesis with internship project

Degree: Master in Industrial Sciences majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Geert Thys (geert.thys@imec.be).

XI. Neuroelectronic Research (NERF)

Introduction

Imec, VIB (Flanders' leading life science institute), and the Leuven University have set up a joint basic research initiative to unravel the neuronal circuitry of the human brain: Neuroelectronics Research Flanders (NERF). Supported by the Flemish Government, NERF looks into fundamental neuroscientific questions through collaborative, interdisciplinary research combining nanoelectronics with neurobiology. It intends to push the boundaries of science, by zooming in on the working of neurons at an unprecedented level of detail. In the long run, NERF will generate new insights in the functional mapping of the brain, as well as research methodologies and technologies for medical applications, i.e. diagnostics and treatment of disorders of the central and peripheral nervous system. The NERF labs are located at the imec premises. Read more: http://www.nerf.be/.

Using virtual reality to study the function and neural circuits in the mouse visual system

The main aim of the lab is to understand the fundamental principles underlying the function of neural circuits during behavior. Towards this goal we investigate how sensory information is processed along the neural pathways that generate visually guided behavior. The lab uses two-photon calcium imaging, high-density probe recordings, optogenetics and computer based analytical methods of neural activity in awake behaving animals. Using these techniques, we study the activity of genetically defined neural populations in response to visual stimulation and perturb components of these circuits to understand their function in visual processing and visually guided behavior. Ultimately, the experiments are designed to understand the fundamental principles of sensory information processing in the brain. The visiting students are expected to have a decent background in computer programming and and instrumentation. Together With the visiting student we will aim to build and use a virtual reality system that will allow us to record neural activity while the animal performs visually guided tasks, i.e. plays a video game. These experiments will allow us to investigate the processing of visual information with and without sensory feedback.

Type of project: Thesis or thesis with internship project

Degree: Master's degree

Responsible scientist(s):
For further information or for application, please contact Karl Farrow (Karl.Farrow@nerf.be).

Acoustic-neuron interaction study in simple animal model

Recent developments in nanotechnologies and neuron science allow nowadays considering the development of high definition refined brain interfaces with therapeutic, relaxation or entertainment applications. Various more or less invasive modalities are competing in this context. They rely for example on electric, magnetic, optical, acoustical signals to address and stimulate brain zones. However, several of these stimulation principles lack yet thorough understanding.
Imec and NERF develop technologies to improve the understanding of brain functions and their interactions with external stimuli. In this context, this thesis targets improving the understanding of the processes involved in the acoustic stimulation of neurons and synapses. The student will work on and develop in vitro and in vivo system models to assess the frequencies, modulations, intensities and repetition rates for these stimulations. For this reason, we look for candidates with affinity for experimental work, with both biological (animal) and technological (acoustic transducer) systems. Basic knowledge of neuron signaling and function as well as basic understanding of acoustic waves and beam forming are required and will be further developed in the course of the thesis.

This thesis will give you the opportunity to learn about an emerging research domain that promises to revolution the life of patients and to get exposed to practical experimental work in nano-bio engineering. It is a perfect extension of your academic curriculum towards solving practical problems.

Type of project: Thesis or internship project or combination of both

Degree: Master in Science and Master in Engineering majoring in physics, bioscience engineering, nanoscience & nanotechnology, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Sebastian Haesler (sebastian.haesler@nerf.be) and Xavier Rottenberg (Xavier.Rottenberg@imec.be).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