Master Thesis & Internship Projects @ imec

2017 Topic Guide

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Information

Students from universities and engineering schools can apply for a Master thesis and/or internship project at imec. Imec offers topics in engineering (technology) and sciences in different fields of research.

All Master internship and thesis projects currently available at imec are collected in this topic guide. The projects are classified according to the imec expertises. You can find more detailed information on each expertise on www.imec.be. In addition, in this catalogue you will find the projects available with imec.IC-link and NERF (www.nerf.be)

How to apply?

Send an application email including your motivation letter and detailed resume to the responsible scientist(s) mentioned at the bottom of the topic description you choose.
The researcher(s) will screen your application and let you know whether or not you are selected for a project at imec.
It is not recommended to apply for more than three topics.

There is no application deadline. We accept applications at any time and deal with them throughout the year.

Master internship students usually receive an allowance. However, some research groups only accept self-supporting students. Do you want to know upfront whether the project you wish to apply for provides financial support? When sending in your application email then check the remuneration details with the responsible scientist. For some projects, it is already mentioned in the project description that an allowance will not be provided.

For more information, go to the Master thesis & internship section on the Work at imec tab on www.imec.be. Do you have additional questions, then send an email to student@imec.be.

For Master thesis/internship projects in **imec the Netherlands** refer to
http://www.holstcentre.com/careers/thesis-opportunities or contact talent@imec-nl.nl.

After acceptance

In case of acceptance to our internship program you are bound to embark on a very exciting and interesting experience! For imec, your contribution as a student will be essential in meeting the deliverables in our programs. Therefore, it is vital that - once you accept to come to imec - we can count on your commitment and dedication for the entire duration of the internship period.

I. CMOS & beyond CMOS

3D interconnect-based segmented bus architecture modelling and exploration

The communication and memory organisation in internet gateways and servers are a major source of energy consumption. Future technologies will lead to higher performances but also to an increased energy bottleneck. In this thesis, we want to build an exploration framework for comparing different 3D interconnect-based options for emerging processor and memory communication architectures. The main goal will be to reduce the overall energy consumption for given application workloads executed on this communication and memory architecture. Simulations will be performed based on available measurement data to calibrate the energy and performance models.

Profile: Strong interest in architecture exploration and simulation, basics of microelectronic technologies with emphasis on 3D interconnect schemes

Type of project: Internship project of 6 months (full-time, at imec Leuven)
The start date of the project is Q2/Q3, 2017

Degree: Master in Engineering majoring in computer architecture or micro-electronics

Responsible scientist(s):
For further information or for application, please contact Eric Beyne (Eric.Beyne@imec.be) and Francky Catthoor (Francky.Catthoor@imec.be).

Organic polymers for microbumps passivation

In order to increase the density of memory chips and improve the performance of logic devices beside scaling electronics devices, 3D integration is also necessary. Microbumps are interconnects between two stacked chips to make connection between them. Increasing density of interconnects or reducing pitch of microbumps in 3D integration to improve the performance of final product, requires new UBM (under bump metallurgies) materials and solder, cleaning and passivation options. The student will study cleaning and passivation of different UBM materials specially BZT organic polymers and their influence on IMC formation (intermetalic compounds) through papers and experimental results. Characterization techniques such as XPS, AFM, Contact angle, ... will be used in this study. 3D stacked chips will be analyzed using cross section, SEM and EDS analysis. Results will be presented in imec PTW weeks and then external conferences or journals.

Type of project: Thesis project

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Electrotechnics/Electrical Engineering, Materials Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Jaber Derakhshandeh (Jaber.derakhshandeh@imec.be).

Sub-nano engineered magnetic tunnel junction stacks for STT-MRAM applications

Future memory technology nodes will require faster, smaller, and more power-efficient devices. Since the conventional memories such as dynamic random access memory (DRAM) and static random access memory (SRAM) are reaching their scaling limits, new emerging memories are being developed. The perpendicular spin- transfer torque magnetic random access memory (STT-MRAM) is considered as a promising replacement. A high performance STT-MRAM stack contains up to 20 different layers, each of them around 1 nm or below. The key component of this memory is the perpendicular magnetic tunnel junction (p-MTJ) consisting of a CoFeB/MgO/CoFeB trilayer in which the CoFeB layers have a (001) texture lattice matched with MgO in order to obtain a high tunnel magnetoresistance (TMR) ratio and interfacial perpendicular anisotropy (PMA). Next to that, a variety of materials is being employed or evaluated in STT-MRAM stacks, each of them for a specific functionality. Co, Pt, Pd, Ni are being used in Co/Pt, Co/Pd, or Co/Ni multilayers as perpendicular synthetic antiferromagnets (p-SAF) for the pinning of the magnetization of one of the CoFeB layers [1-3].
The commonly used method to fabricate the STT-MRAM stacks is physical vapor deposition (PVD) in a cluster set-up where all layers can be deposited without air exposure. The impact of the impinging atoms on the substrate during PVD deposition needs to be studied and controlled [1]. In the case of ultrathin films in the 1-nm range commonly used in STT-MRAM stacks, sub-monolayer damage is no longer negligible since its functionality relies on interface effects such as interface induced PMA. From that perspective, preventing interface damage during deposition of a large atom, such as Ta, on top of a lower density material, such as CoFeB, is highly challenging, and can potentially limit the use of the material, despite its many advantages. Controlling the interface roughness and thickness is also required to enable the compatibility of the STT-MRAM stack with the high thermal budgets up to 400 °C that are applied when the stack is integrated into a CMOS process flow.
The student will conduct an experimental study of the impact of the impinging atoms during PVD deposition on the magnetic properties of sub-nm thin ferromagnetic films that are used in perpendicular STT-MRAM stacks aiming to improve the magnetic tunnel junction performance. Furthermore, in-situ annealing and cryogenic cooling will be investigated to improve further their structural and magnetic properties such as perperdicular anisotropy and tunnel magnetoresistance. The films will be deposited on 300 mm Si wafers using an industry relevant PVD multi-target cluster tool. Magnetic and electrical characterization is done by vibrating sample magnetometry, Kerr magnetometry, and current-in-plane tunneling. X-ray reflectivity, X-ray diffraction, SEM, TEM, rutherford backscattering will be used for structural characterization.

References:
Swerts et al., Appl. Phys. Lett., 106, 262407 (2015).
Tomczak et al., Appl. Phys. Lett., 108, 042402 (2016).
Devolder et al., Appl. Phys. Lett., 108, 172409 (2016).

Type of project: Internship project with a minimum duration of 4 months or thesis project with a minimum duration of 6 months, but preferably 12 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Materials Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Johan Swerts (Johan.Swerts@imec.be) and Sebastien Couet (Sebastien.Couet@imec.be).

Study of the kinetics of chemical reactions in nanostructures

In semiconductor manufacturing, new generations of devices have entered the nano-world, with critical dimensions smaller than 100 nm. Many process steps are still performed using aqueous chemistries, e.g. wet etching of materials for patterning and wet cleaning of surfaces. New transistor geometries are vertical, with the generation of 1-D and

2-D nano-confined spaces (Fig. 1). Little is known about the kinetics of chemical reactions in nano-confined volumes. Chen et al. (2009) showed that the rate of enzymatic reactions was increased in nano-vesicles, while Okuyama et al. (2015) obtained a decreased etching rate for 1-D confined SiO2 nano-layers. Mechanisms affecting reaction kinetics at the nano-scale are not well understood. Chen et al. (2009) suggested that both an increased enzyme-substrate collision frequency and the enzyme-vesicle wall interactions may affect the reaction rate, while Okuyama et al. (2015) proposed that surface charges affected the concentration of reactive ions in the nano-slit.
In this project we investigate the kinetics of chemical reactions in nano-holes with 2-D confinement (Fig. 2). In a first part the etching behavior of metallic layers covering the wall of nano-holes with varying diameter will be studied (e.g. TiN using ammonia-hydrogen peroxide mixtures). The student will perform the wet etching tests, the data treatment of TEM (transmission electron microscopy) pictures generated by operators in the pilot-line, and a kinetic analysis. Results will be compared to etch rates obtained on planar films with film thickness measured by ellipsometry. In a second part the kinetics of reactions involving a SAM (self-assembled monolayer) deposited on the structures will be studied using ATR-FTIR (attenuated total reflection Fourier-transform IR spectroscopy). The method has already been developed and tested on nano-lines with 1-D confinement, where a rate increase of 30% was observed. Here the student will prepare the ATR crystals (polishing), perform the FTIR tests using a home-build liquid cell, as well as the data treatment and interpretation. The content of the student project will be adapted depending on the progress of our research.

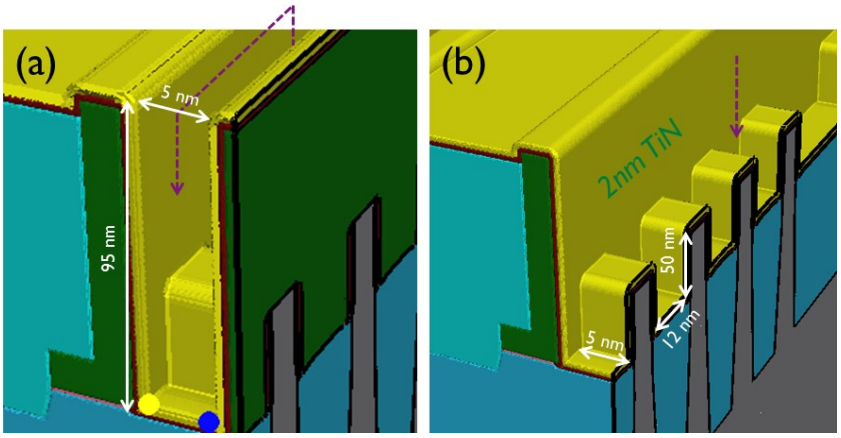


Figure 1. Cross-sections in a cartoon of a FINFET transistor after removal of the dummy gate (not to scale), showing (a) a nano-slit with 1-D confinement, (b) nano-holes with 2-D confinement.

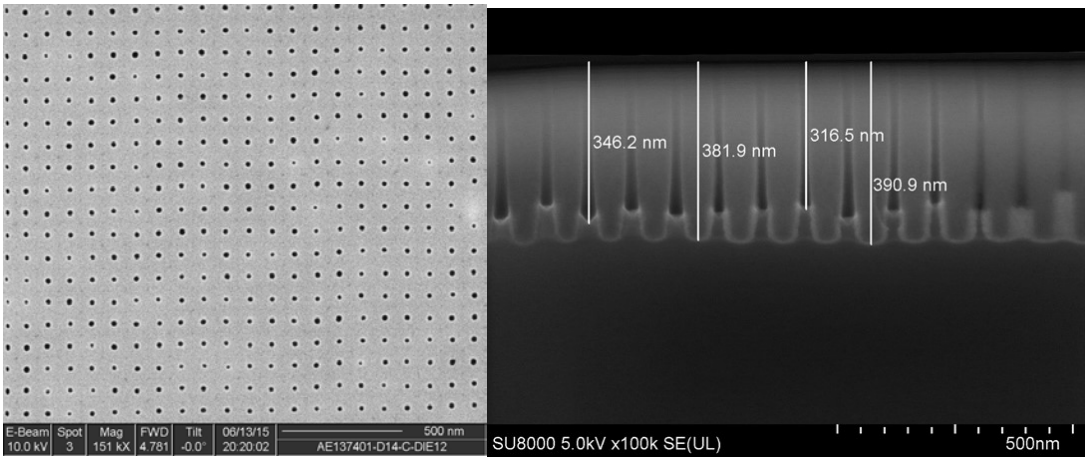


Figure 2. SEM images of nanoholes: (left) top view, (right) cross-section view.

Type of project: Internship or thesis project or combination of both with a minimum duration of 3 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Guy Vereecke (Guy.vereecke@imec.be).

Novel spin-on method to deposit self-assembled monolayers and thin polymeric films for surface and interface engineering in nano-IC applications

As the total transistors and interconnects sizes come down to few tens of nanometers and below, a shift in paradigm for the manufacture and integration of microelectronics components becomes apparent. Organic molecules - owing to their size, mechanical flexibility and chemical tunability - fit well in this slot and, thus, are expected to play a key role in IC downscaling. In this respect, self-assembled monolayers (SAMs) seem the best candidates. SAMs are a prototypical form of nanotechnology: the SAM precursor molecules carry the "instructions" required to generate an ordered, nanostructured material without external intervention. SAMs demonstrate that molecular-scale design, synthesis, and organization can generate macroscopic materials properties and functions. Although the details of the thermodynamics, kinetics, and mechanisms of assembly will differ significantly, these monomolecular films establish a model for developing general strategies to fabricate nanostructured materials from individual nanometer-scale components. Because SAMs can assemble onto surfaces of any geometry or size, they provide a general and highly flexible method to tailor the interfaces between nanometer-scale structures and their environment with molecular (i.e., subnanometer scale) precision. SAMs and polymeric films can control the wettability and electrostatic nature of the interfaces of individual nanostructures and thus their ability to organize into large assemblies and interact with overlayers adding chemical functionality, thermodynamic stability. While deposition on SAMs by dipping is already being extensively studied, thiol SAM spin-on from organic solvents is relatively unexplored. The first phase of this project will focus on the deposition and characterization (water contact angle, FTIR, XPS, AFM, ..) of thiol SAMs and eventually functionalized polymeric films on metal surfaces by spin-on from organic solvents. The study includes metal surface preparation before SAM deposition and the impact of post-SAM treatments such as anneal, gas flow and/or wet chemistries. The final aim of this work is to achieve a dense, ordered and defect-free SAM.In the second phase of the project we will focus on the scale-up of the SAM deposition process to 300mm wafers and on 300mm scale metrology techniques, such as light scattering, AFM, ellypsometry, mass measurement.

Type of project: Internship or thesis project or combination of both with a minimum duration of 6 months, but preferably 12 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Materials Engineering

Responsible scientist(s):
For further information or for application, please contact Silvia Armini (armini@imec.be).

Machine learning based computational lithography

As the chip scaling continues technology node to node to follow Moore's law, computational jobs such as optical proximity correction (OPC) and design-for-manufacturability (DFM) have become too intensive to carry out with introduction of more design data and models (mask, optical, resist, etch, topography-aware and CMP) to improve chip printability and prediction accuracy. 'Big Data' usually refers to data volumes that are so large that traditional data processing applications are inadequate, which exactly represents current OPC and DFM confront. In consequence, increased risk with increased ramp-up time from research to high volume manufacturing has been

pointed out as risk as well as risks. The student will learn conventional OPC and DFM flow and work toward developing and applying "Machine learning" and optimization algorithms into OPC and DFM flow as a goal to 1) reduce number of iteration, 2) reduce computational resource and 3) optimize/minimize DOE to shorten turn-around-time (TAT) in early develop and yield ramp up in Semiconductor manufacturing. Machine learning and optimization may include study of

- Pattern recognition (layout pixilation), Pattern extraction, Classification
- Machine learning Modeling - training using optimization algorithm. Optimization incorporates mathematical and statistical concepts (effect, global/local min. search algorithm), or a new concept.

Type of project: Internship or thesis project or combination of both with a minimum duration of 6 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Computer Science, Electrotechnics/Electrical Engineering, Nanoscience & Nanotechnology, Physics

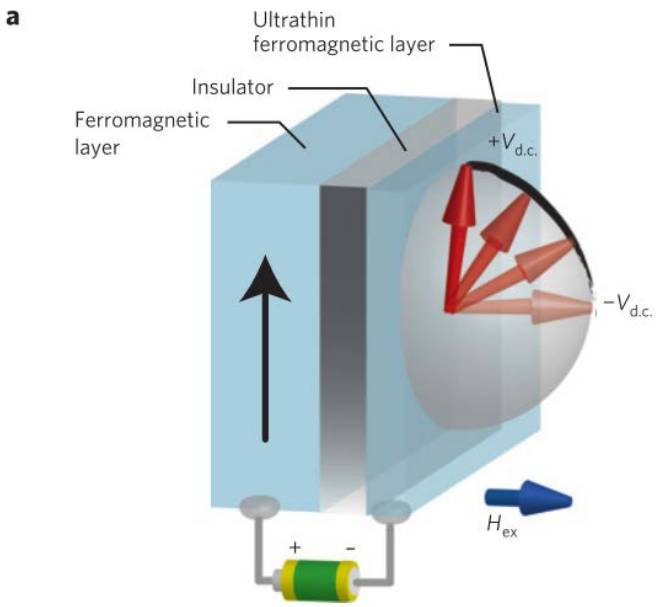
Responsible scientist(s):
For further information or for application, please contact Ryan ryoung-han kim (Ryan.ryoung.han.kim@imec.be) and Jae Uk Lee (Jae.uk.lee@imec.be).

The giant Voltage Control of Magnetic Anisotropy (VCMA) effect for enabling next generation spintronics and magnetic memories

The dynamic control of magnetic materials using an electric field enables key applications in the fields of magnetic memories (MRAM), and spin-based logic. In particular, the possibility to modulate the magnetic anisotropy of a ferromagnetic metal using VCMA [1] has the potential to decrease the energy consumption of magnetic technologies by several orders of magnitude. However, the currently achieved magnitude of the VCMA effect is not sufficient for a groundbreaking application.
In this project, the student will explore one of the two following aspects of VCMA, depending on the available experimental material and their inclination:

- the optimization of the VCMA effect, through engineering the materials and the interfaces involved in VCMA or;
- the applications of the VCMA effect in spin-based logic, through micromagnetics simulations and electrical characterization of devices.
- In both cases, the student will work with specialized materials, techniques and tools to meet the requirements of this advanced topic.

[1] Maruyama et al., Nature Nanotechnology, 4, 158 (2009)



[Figure] Nozaki et al., Nature Physics, 8, 492 (2012)

Type of work: The work will consist of 10 % literature study and 90 % experimental and modeling work.

Type of project: Thesis project

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Electrotechnics/Electrical Engineering, Materials Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Bart Vermeulen (Bart.vermeulen@imec.be) and Koen Martens (Koen.martens@imec.be).

In-situ electron beam study of fracture events to assess the strength and compliance of advanced BEOL structures at the nanoscale

Chip-package interaction is a critical reliability issue for Si microelectronics chips with Cu/low-k Back-End-Of-Line (BEOL) interconnects. Package processing causes high vertical and shear forces to the thin BEOL layers, which might result in fracture or delamination. As the technology advances, the interconnect structures continue to evolve with decreasing dimensions, increasing porosity of intermetal dielectrics and an increasing number of layers and complexity. The introduction of advanced materials on both chip and package level and the harsh environmental conditions during processing and operational use cause additional challenges for reliability analysis and prediction. In the microelectronics industry, current materials selection is made with limited understanding of elastic properties, fracture properties and interfacial adhesion of thin continuous films deposited on a silicon substrate. However, these parameters do not sufficiently represent the failure behavior and structure stability of multilevel interconnects, where each material exist as an individual part with different shapes and various cross-section geometries. To gain more insight into root causes of failure processes, the semiconductor industry needs reliable, reproducible testing methods and strategies to monitor these parameters, not only for low-k dielectric films, but also for complete interconnect stacks. Therefore, a careful characterization of the mechanical stability of potential new low-k candidates is required to integrate these new materials and Cu interconnects and assure reliability during chip packaging and under field conditions. To capture the fracture onset and crack propagation, high-resolution real time techniques are preferred over post mortem observations. Electron beam based methods are one of the most

commonly used techniques for in-situ studies, since they yield a high lateral resolution without additional specimen preparation. The focus of this work lies on the development and application of new in-situ nanoindentation and electron beam based mechanical test methodology to assess the strength and compliance of BEOL structures at the nanoscale and to provide quantitative data that can be used to determine allowable chip/package interactions. The master student will work on: definition of test structures (ex. films, beams or pillars), sample preparation and mounting in a SEM or nanoindenter, application of mechanical forces inside the SEM or nanoindenter on the test structures and monitoring in-situ the effects (force-displacement and crack formation), scientific analysis of the results.

Type of project: Thesis project

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Materials Engineering, Mechanical Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Kris Vanstreels (Kris.vanstreels@imec.be), Ingrid De Wolf (Ingrid.dewolf@imec.be) and Jin Won (Maria) Seo (Maria.seo@kuleuven.be).

Full-zone band structure calibration for the quantum mechanical simulation of confined III-V TFETs

As scaling of semiconductor components enters the nanometer regime, the increase in power density becomes an important bottleneck. The root cause lies with the 60 mV/dec limit on the subthreshold swing of a classical MOSFET, which causes large leakage currents if the supply voltage is scaled too aggressively. Alternative transistor concepts, based on quantum mechanical tunneling, are able to circumvent the subthreshold swing limit thanks to their different current injection mechanism. Among the most promising concepts in this category is the tunnel-FET (TFET). The TFET relies on band-to-band tunneling, which allows for sub-60mV/dec subthreshold swing and low leakage currents. To obtain sufficient ON-currents, TFET research is focusing on III-V materials, which exhibit a wide range of effective masses and bandgaps.
To model this new type of transistor and the new material systems, accurate quantum mechanical simulation tools are required. At imec, we have therefore developed Pharos, a quantum simulator for III-V TFETs. Pharos relies on a band structure calculated with the k.p method. It is the first such simulator that captures the full first Brillouin zone. This full-zone capability is especially important when investigating very confined structures, such as nanowires. However, there is a lack of reliable full-zone k.p parameters in literature, which limits the applicability of the simulator in confined structures.
The goal of this thesis project is therefore to obtain a calibration procedure for k.p band structures of III-V materials and to use the calibrated parameters to simulate confined TFET structures. After gaining proficiency in the k.p band structure method, the student will carry out a full-zone calibration of k.p band structures to an ab-initio reference for several relevant III-V materials. The student can start from an existing rudimentary algorithm. The goal is to obtain a calibration procedure that is transferable to other materials as well. Once calibrated parameters have been obtained, the student will use imec's in-house developed quantum simulator Pharos to investigate strongly confined TFET structures. He/she can then assess the utility of the calibrated band structures in the design of next generation TFETs.
For this challenging topic a good knowledge of semiconductor physics and semiconductor devices is required, as well as a solid background in quantum mechanics. The research will be carried out in the TFET team at imec, which has extensive experience in characterization and quantum mechanical modeling of tunneling-based devices.

Type of project: Thesis project

Degree: Master in Science and Master in Engineering majoring in Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Devin Verreck (verreck@imec.be).

Surface chemistry and atomic layer etching of III-V semiconductors for 5 nanometer CMOS technologies and beyond

The ultimate scaling limit of Si-based complementary metal-oxide semiconductor (CMOS) technology is rapidly approaching. Despite the excellent properties of the group IV semiconductor and its native oxide, the continued reduction of the dielectric oxide thickness has necessitated the use of high-k gate dielectrics and a metal gate. At present, the performance enhancement for Si-based transistors can no longer be guaranteed due to intrinsic mobility issues. The considerably higher mobility of III-V compound semiconductors (i.e. InGaAs, InAs, InSb) has led to renewed interest and a following phase in the development of extremely scaled transistors for 5 nm technology nodes and beyond. Wet-chemical treatment (e.g. for layer selective etching, surface and interface passivation, removal of native oxides, channel trimming, etc.) are an essential part of device fabrication. Due to the very small transistor dimensions etching selectivity and control at the (sub)atomic-layer-scale is required. In order to design wet-chemical etchants that can be used for this purpose, insight in the interactions between surface atoms and molecules in chemical solutions is required. For atomic layer etching, a kinetically controlled dissolution reaction is preferred, because hydrodynamic conditions are generally more difficult to control. Semiconductor dissolution processes are known for their complexity. Charge transfer reactions between valence and conduction band electrons and oxidizing species, chemical interactions, surface states, bond rupture, oxide formation and dissolution all need to be considered in order to obtain fundamental insight in the surface chemical and electrochemical etching process. Apart from (photo)electrochemical etching, two forms of "open-circuit" etching can be distinguished which generally require an oxidizing agent. In chemical etching, valence electrons are transferred directly from surface bonds to the oxidizing agent, giving rise to rupture of the bonds and dissolution of the solid. In electroless etching, the oxidizing agent removes electrons from the valence band of the solid; this is equivalent to injection of holes. The holes are mobile and, if localized in surface bonds, cause bond rupture and dissolution. Such chemical and electroless dissolution mechanisms can have a significant impact on surface properties after chemical treatment. In the former case they can be exploited for surface morphology control while in the latter case non-stoichiometric dissolution can result in build-up of elemental species which may induce undesired electronically active bandgap states detrimental to interface formation. During this internship the main focus will be on the group III arsenides. At present, the surface (electro)chemistry of these semiconductors during atomic layer etching is not well understood. Of special interest is the role of anions on the surface chemical and electrochemical reactions. Careful mapping of parameter space (In/Ga content, acid concentration, redox species, temperature, etc.) will provide insight. A large variety of analytical techniques are available at imec. Inductively coupled plasma mass spectrometry and various electrochemical methods are used to obtain insight in oxidation/dissolution kinetics and stoichiometry. Further mechanistic insight is be obtained by studying the surface chemistry with x-ray photoelectron spectroscopy, photoluminescence, elastic recoil detection, (conductive) atomic force microscopy, profilometry, scanning and transmission electron microscopy.

Type of project: Thesis or internship project with a minimum duration of 4 months

Degree: Master in Science majoring in Chemistry/Chemical Engineering, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Dennis van Dorp (vandorpd@imec.be).

Edge placement error budgeting in CMOS process flow

With the continuous shrink of technology nodes, lithography becomes more and more challenging. At 20 nm node, double patterning technology (DPT) was the usual way of achieving the fine device structures. Until EUV is available as a high volume manufacturing (HVM) solution, DPT or triple patterning technology (TPT) will be required to sustain scaling. However, as the industry goes forward with scaling, for sub-14 nm nodes the chip manufacturers are anticipating three or four masks per layer. Exposing the patterns separately allows the spacing or pitch of the structures to be reduced by a factor of two (or more for triple/quadruple patterning) while increasing the metrology and inspection challenges. As multiple masks are used for patterning one layer, placement of individual layers as well as pattern variations within each layer becomes important for these extremely small structures. To assess these small changes CD-SEM's are used. Starting from standard CD (Critical Dimension) measurement approaches, the industry quantifies the printability performance on wafer based on SEM (Scanning Electron Microscope) pictures and algorithms that determine distances (CD) at specific locations. Once these measurements are acquired, the performance of the lithographic process needs to be evaluated. Position of each pattern is of utmost importance as we scale from node to node. In such a scenario pattern placement error determination is one of the key requirements for assessing the yield of device structures. Determination of this PPE/EPE(edge/pattern placement error) budget for particular process flows needs to be done so that the right process assumptions can be made for particular node.
The purpose of this internship is to come up with an analysis method where we should be able to do EPE budget analysis for the 7nm node and below. Data collected on specific features of interest (contours) need to be evaluated in different ways. At the end of the project we should be able to come up with a tool in Matlab which will help in determination of PPE budgets as well as plot them.

Required skills: MatLab GUI development, programming skills

Type of project: Internship project with a minimum duration of 6 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Electrotechnics/Electrical Engineering, Materials Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Sandip Halder (halder@imec.be), Philippe Leray (leray@imec.be) and Anne-Laure Charley (charley@imec.be).

Automatic recipe and data management development for Fab automation

Background:
For operational excellence of semiconductor fabrication process at pilot line, recipe management is important in order to avoid any human error, such as wrong recipe selection by operator and wrong recipe file naming by engineer. Therefore, a recipe management system needs to be developed to check recipe name and to filter wrong recipe. Not only recipe management, but also data management in metrology tool is critical in order to deliver data to end user. To do so, data management SW needs to be developed.
Task:

1. Development of software and (or) script for recipe list generation and checking recipe name by a recipe name convention rule and filtering recipe against the rule.
2. SW/Script development for data export to a data storage location.

Goal:
Software and script development for recipe management on ellipsometry and for result data management on automatic automic force microscopy.

Type of project: Internship project

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Computer Science, Electrotechnics/Electrical Engineering, Materials Engineering, Mechanical Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Tae-Gon Kim (tae-gon.kim@imec.be).

Atomic layer deposition of metal doped HfO2 as ferroelectric material for future memory technologies

Several metal doped HfO2 deposited by atomic layer deposition have shown ferroelectric behavior making the system a potential choice for 1T and 1T-1C ferroelectric memory solutions [1]. In 2011 it was observed that deviations from the commonly assumed polymorphism of HfO2 or ZrO2 (monoclinic - tetragonal-cubic) is possible with the formation of an intermediate non-centrosymmetric orthorhombic phase having ferroelectric behavior [2]. The concentration of dopant metal (e.g. Al, Si, Gd, Sr) in the HfO2 host can be controlled at the atomic level by dopant: Hf pulse ratio during the self –limiting growth characteristic to the atomic layer deposition process [1]. By using sequential exposures, gas phase reactions between the precursors are avoided and the thin film grows solely by surface reactions. The post-deposition anneal after the deposition of mechanically constraining capping layer(s) triggers formation of orthorhombic phase [1]. The project involves literature study as well as the experimental investigation of doped HfO2 deposition and their physical properties. Post-anneal of the samples will be an important step in creation of the orthorhombic phase. Evaluation of strain induced by the capping layer by ellipsometry will give further understanding how to control the orthorhombic phase formation. The samples will be characterized by techniques such as X-ray reflectivity (XRR), grazing incidence X-ray diffraction (XRD), and grazing angle attenuated total reflectance Fourier transform infrared GATR-FTIR. Dielectric constant and ferroelectric behavior will be evaluated from capacitance-voltage and polarization –voltage measurements. Further analyses, e.g. Rutherford backscattering spectroscopy and atomic force microscopy (AFM) will be performed in collaboration with imec's material characterization group.

1. Michael Hoffmann, Tony Schenk, Ivan Kulemanov, Christoph Adelmann, Mihaela Popovici, Uwe Schröder & Thomas Mikolajick, Low Temperature Compatible Hafnium Oxide Based Ferroelectrics, Ferroelectrics, 480:1, 16-23 (2015).
2. T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, Ferroelectricity in hafnium oxide thin films, Appl. Phys. Lett., 99(10), 102903 (2011).

Type of project: Internship or thesis project with a minimum duration of 6 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Materials Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Mihaela Popovici (popovici@imec.be).

Advanced Source-Drain contact resistance

Throughout the previous decades ever faster, smaller and cheaper computers have revolutionized our life. The main driving force behind this has been the shrinking of the basic building block of digital circuits, the metal-oxide-semiconductor (MOS) transistor. The MOS transistor is a digital switch with a low resistance ON state and a high resistance OFF state, so the channel resistance thus must be kept to a minimum level. Therefore the source and drain contact resistance becomes more and more important in the total source-drain resistance.
The main factors that determine the contact resistance are next to contact area, the actual Schottky Barrier Height and the dopant activation near the interface. The Schottky Barrier Height is not simply related to the contacting

metal work function but suffers from fermi level pinning (FLP). This FLP can be reduced by the introduction of an interfacial layer or other interface treatments, to remove the FLP with minimal resistance introduced.
This module team selects and tests materials and processes on different semiconducting source-drain materials, Si, Ge, SiGe and InGaAs, for n and p MOSFETs, to reduce the contact resistance. Materials and processes are not restricted to those available at imec, but often samples are sent to other companies for special processes. E.g. hot or cryogenic implantations and laser treatment are used to increase the concentration of activated dopants. Special film deposition and thermal treatments are used to reduce the contact resistivity further. A simple test structure is the work horse to allow fast screening; the processing and electrical analysis were optimized to maximize the performance. Often, after initial electrical analysis a wafer is cut into serval coupons which can each be given a thermal treatment and are measured again afterwards.
The emphasis of this work is on electrical measurement of these contact structures and on analysis of the electrical data, together with the team, to link the electrical data to the experimental variations and build understanding of the relation between physical and electrical properties. Another output of this work is to select materials with optimal properties from these screening experiments, for application at contacts in advanced devices.

Type of project: Thesis project with a minimum duration of 6 months

Degree: Master in Engineering Technology and Master in Engineering majoring in Electrotechnics/Electrical Engineering, Materials Engineering, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Marc Schaekers (Marc.schaekers@imec.be).

3D chemical analysis of microelectronics systems

One driver of the semiconductor industry growth is the sustained realization of "Moore's Law", whereby the number of transistors in an integrated circuit doubles approximately every 2 years with an associated increase in circuit functionality, reduction in operational power, and, most important, a reduction in unit cost. These fast technological developments, including increased process and material complexity, as well as reduced tolerance levels for process excursions have increased the need for a more controlled manufacturing environment necessitating equivalent improvements and developments in metrology. The present evolution towards merging lab and Fab metrology implies that these developments are necessary for use both in the R&D phase as in the final production phase. 9 With the strong size dependence of many material problems and phenomena, metrology needs to be performed more and more on devices with realistic dimensions and on wafer scale. Imec has recently acquired a new metrology tool combining a TOF-SIMS (Time of Flight Secondary Ions Mass spectrometry) and an AFM (Atomic Force Microscope) instrument. This instrument is designed in order to combine chemical information from the TOF-SIMS with topographical information from the AFM, allowing 3D chemical mapping of samples. The objective of this thesis is to establish this AFM/TOFSIMS system as a 3D-metrology tool. For this objective, the AFM module will be used purely in topographic mode. The first part of the thesis will be devoted to the qualification of this new instrument to establish its ultimate performances, before applying it to model system. These systems will be chosen from technologies from the BackEnd-OF-Line (dual damascene). In these systems, etching of trenches occurs via a Reactive Ion Etching step, leaving polymer residues on the structures. These residues need first to be cleaned before metal deposition can occur and a detailed chemical analysis is frequently needed to determine the optimum cleaning process and its efficiency. This can be evaluated by XPS on specifically designed structures . However, the information content of TOFSIMS for organic contaminants is much higher than from photoemission, hence TOFSIMS is a preferred analysis approach. Unfortunately, the topography on the line arrays prevents a full 3D reconstruction of TOFSIMS profiles. The application of the 3D-TOFSIMS system using the in-situ AFM represents an important step forward in this case. After filling the trenches with Cu, one still has no or limited physico-chemical information on the 3D Cu concentration in the ILD between Cu lines. A prominent challenge one faces in analyzing these structures, is that when using sputtering for depth profiling, topography is developing during the analysis due to large difference in erosion rate between the different materials. This thesis will show that this problem can be solved using TOFSIMS-AFM by monitoring the topography growth and implementing correction procedures. The output will be protocols for quantitative composition profiles for heterogeneous and non-planar systems.

Type of project: Thesis with internship project with a minimum duration of 6 months

Degree: Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Materials Engineering, Physics

Responsible scientist(s):
For further information or for application, please contact Alexis Franquet (Alexis.Franquet@imec.be), Thierry Conard (Thierry.Conard@imec.be) and Valentina Spampinato (Valentina.Spampinato@imec.be).

Atom Probe Tomography for future 3D metrology applications

The enhancement in semiconductor device performance has for many years been readily achieved through device scaling i.e. the fabrication of smaller devices. However, this approach is becoming more challenging and to meet the semiconductor roadmap, alternatives to complement scaling are being explored. These involve the use of semiconducting materials other than conventional Si and include SiGe, Ge, GaAs, InGaAs, GaN, InP, etc. Moreover, there is also a significant move away from planar i.e. 2D, device architecture towards 3D device structures. These changes mean that the metrology used for quantifying such structures also needs to adapt. Laser assisted Atom Probe Tomography (APT) is one technique which could provide the 3D quantitative analysis required with an excellent sensitivity (10 ppm) and near-atomic spatial resolution (~0.2-0.3 nm). In simple terms, APT exploits the concept of field evaporation and ionization of atoms from the apex of a needle-shaped specimen (~50 nm tip radius) and their projection onto a position sensitive detector. By taking the reverse projection of the detected ions, a tomographic reconstruction of the specimen is obtained and a full 3D quantitative analysis achieved. However, as the technique is still in its infancy for semiconductor materials, there are numerous challenges still to be overcome. This will only be achieved through a better knowledge into the underlying physics of the technique e.g. laser-sample interaction, tip heating and atom migration etc. The objective of this internship/master's thesis is therefore twofold; to join a research team currently working on addressing the underlying physics facing APT by analyzing the semiconductor materials (and their combinations) of tomorrow (e.g. compounds, oxides, heterogeneous materials) with the objective of establishing a fundamental understanding of the measurement artefacts, their root causes and determining a means to correct for them. Secondly, it offers an excellent opportunity to gain experience and an insight into state of the art scientific instrumentation (e.g. focused ion beam secondary electron microscopes and two APT instruments) and the semiconductor materials being developed for future technology. Due to the ongoing activities of the team, a more detailed project of research (or options depending on the situation) will be outlined closer to the time.

Type of project: Internship or thesis project or combination of both with a minimum duration of 6 months

Degree: Master in Science and Master in Engineering majoring in Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Richard Morris (richard.morris@imec.be), Claudia Fleischmann (claudia.fleischmann@imec.be) and Janusz Bogdanowicz (Janusz.bogdanowicz@imec.be).

Seeding and growth of boron-doped diamond thin films

Diamond is outforming other materials in many domains such as hardness, wear resistance, thermal conductivity, chemical inertness, and biocompatibility. As it can be made electrically conductive (p-type) by boron doping, boron-doped diamond thin films look especially attractive for electrical applications. They are being explored and developed for a wide range of applications including chemical treatment (e.g. waste water, swimming pool, chemical solutions), nanoscale electrical probes, implantable bio-electrodes, and water splitting/hydrogen generation.
The goal of this internship is to obtain better insight into the interfacial growth of boron-doped diamond layers. For this, the student will seed and grow diamond layers using imec's hot-filament chemical vapor deposition (HFCVD) reactor using different doping levels, seeding densities and growth parameters. The electrical analysis at the nanoscale

is carried out on the interfacial side using electrical AFM methods such as SSRM and conductive AFM (c-AFM) for studying the grain and grain-boundary conductivity. Here, we look for a correlation between boron doping level and grain conductivity. Furthermore, a comparison of doped versus undoped diamond seed nano-crystals is done. The conversion of a seed layer into a highly conductive interfacial layer is not completely understood yet and is therefore investigated in detail in this study. For physical analysis, scanning electron microscopy (SEM), RAMAN, and elastic recoil detection (ERD) are used.
For this topic, the student will work inside a lab and cleanroom environment to carry out the required experimental steps. The student will characterize the fabricated samples by different characterization techniques. The student will be part of imec's materials and component and analysis group.

Type of project: Internship or thesis project or combination of both with a minimum duration of 6 months

Degree: Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Electrotechnics/Electrical Engineering, Materials Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Thomas Hantschel (Thomas.Hantschel@imec.be).

Electrical SPM for the analysis of magnetic memory

Spin-transfer torque magnetic resistive memory (STT-MRAM), is emerging as a potential replacement for Flash and/or DRAM applications, as they exhibit non-volatility, high-speed, low-voltage switching and almost unlimited read/write endurance. However, significant challenges toward the widespread commercialization of this technology are still in the area of process scaling, materials integration and physical operative mechanisms. In this context, electrical scanning probe microscopy (SPM) techniques such as (C-AFM, KPFM and SSRM) represent invaluable tools for the analysis of post-patterning treatment and material selection in magnetic tunnel junctions, as they allow the probing of nanoscaled features. This internship/thesis fits into the characterization framework for STT-MRAM using a set of electrical SPM techniques. You will be trained in the use of the tool and you will intensively use it focusing on device characterization methodologies. During the period of the internship the student will focus particularly on material characterization and AFM-analysis. The data analysis and interpretation will cover an important part of the work; you will apply statistical principles in data collection and will be asked to rule out your results. You will work in an international R&D team; a good command of English language is required. The detailed content of the work will be defined in detail at the moment of starting this project.

Type of project: Internship or thesis project or combination of both with a minimum duration of 6 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Electrotechnics/Electrical Engineering, Materials Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Umberto Celano (Umberto.Celano@imec.be).

Advanced analysis of Rutherford backscattering spectrometry through parallel processing

This work will be executed at imec, which is the leading European micro-electronics research center. Imec does research on a wide variety of front edge micro-electronic devices and applications (transistors, memories, solar cells,...). To verify the correct fabrication of these extremely challenging new devices (sub-22 nm technology) also

high end characterization tools are essential. In this framework accelerator based characterization is one of the approaches that is pursued. For this, imec operates a 2 million Volt tandem particle accelerator, connected to multiple beam-lines and detection end-stations (vacuum chambers) maintained at high vacuum. The experimental results (spectra) are compared to physical models to quantify the properties of the fabricated devices.
As of now, the optimization of the model towards the experimental result is achieved by least squares fitting (fitting) using the grid-search or Levenberg-Marquardt algorithm. In this scheme, due to the computational demand, only a few parameters can be fitted (at once), and the analyst needs to supervise and steer the analysis constantly – a lengthy and labor intensive activity.
The purpose is develop a new software program for the analysis of the experimental results. We will implement new algorithms for the optimization that lend themselves better towards parallelization, for example the differential evolution algorithm. Besides, the student will also prepare the necessary code to allow for parallel operation on multiple cores and demonstrate its advantages.
The main tasks will be:

- To implement alternative optimization algorithms, for example the differential evolution algorithm.
- To investigate the performance of the new optimization method.
- To prepare the new program to allow its execution on multiple cores.

This subject is an opportunity for those who wish to get in-depth experience in "Big data" analysis strategies. Meanwhile, the student will gain practical experience with multi-core and parallel processing and on computational optimization.

Type of project: Thesis project or thesis combined with internship project with a minimum duration of 6 months

Degree: Master in Science and Master in Engineering majoring in Computer Science, Physics

Responsible scientist(s):
For further information or for application, please contact Johan Meersschaut (Johan.Meersschaut@imec.be).

Embedded distributed human-machine application for accelerator based metrology

This work will be executed at imec which is the leading European micro-electronics research center. Imec does research on a wide variety of front edge micro-electronic devices and applications (transistors, memories, solar cells,...). To verify the correct fabrication of these extremely challenging new devices (sub-22 nm technology) also high-end characterization tools are essential. In this framework accelerator based characterization is one of the approaches that is pursued. For this, imec operates a 2 million Volt tandem particle accelerator, connected to multiple beam-lines and detection end-stations (vacuum chambers) maintained at high vacuum. Continuous and ongoing improvements and investments to the detection systems and the control software allow us to be internationally at the forefront regarding ion-beam based metrology for microelectronics applications.
This subject involves the implementation of a distributed embedded control application (WASP) to enable the accelerator based metrology at imec. This project aims at the development of a new software package for the control of the system in a modular and naturally multi-threaded concept. In particular, the software allows to communicate with single devices through Ethernet (TCP/IP) and RS232/RS485 (via Serial-Ethernet gateways) and with the user through a user-friendly graphical interface (GUI) as well as support for a flexible scripting language capability.
The new software architecture is designed such that new devices can be connected and disconnected dynamically during the operation, and the devices appear as virtual instruments on the screen. The signals from various virtual instruments are accessible to both the GUI as well as to scripts that can be run in a command-like environment.
The WASP concept was originally designed to control the hardware and data acquisition. However, the concept potentially may also be very powerful and useful to realize an on-line data analysis. The algorithms to perform the data analysis are available, but at this moment the analysis has to be manually initiated and supervised by the analyst.
The main tasks will be:

- To implement communication drivers, so-called daemons or services, (with stepper motors, data acquisition, counters, data analysis routines) in the Visual C++ environment using WinForms.

- To implement a graphical user interface in HTML + Javascript to run with Windows' Hypertext Application environment (HTA)
- To implement the same functionalities in Javascript to run in the console with node.js

This subject is an opportunity for those who wish to experience the aspects of programming in C/C++, Javascript, HTA, and node.js based environment for the development of human-machine interfacing and automation.

Type of project: Thesis project or thesis combined with internship project with a minimum duration of 6 months

Degree: Master in Engineering Technology majoring in Computer Science

Responsible scientist(s):
For further information or for application, please contact Johan Meersschaut (Johan.Meersschaut@imec.be).

One-dimensional carrier profiling of blanket and confined semiconducting structures

The performance increase of Complementary Metal Oxide Semiconductor (CMOS) devices at every new technology node has required to shrink their dimensions to the nanoscale and to introduce new high-mobility channel materials (Ge, SiGe, III-V). More recently, these devices have also moved from planar to three-dimensional architectures. In this context, it is urgent to develop a characterization technique able to accurately determine the incorporation and activation of dopants in the ultra-shallow doped regions of the transistors, i.e. the source, drain and extensions. This project aims at tackling this critical issue by combining two established techniques, i.e. Secondary Ion Mass Spectrometry (SIMS) and microhall (MH). SIMS is the established technique for one-dimensional dopant profiling. In a nutshell, SIMS is based on the layer-by-layer sputtering of the sample with the help of a low-energy ion beam. The fraction of the sputtered atoms which are ionized is accelerated by an electric field to a mass spectrometer, where each species is separated and counted. Unfortunately, SIMS does not capture any electrical information about the sample as it measures the total dopant profile, i.e. including the inactive portion. In this project, we propose to incorporate multiple MH measurements during the sample sputtering to determine the active doping concentration at different stages of the profiling. This project will essentially consist of two tasks. Task I will deal with simple blanket structures of doped Si and more advanced SiGe, Ge and III-V materials. MH measurements will be run either on the sputtered surfaces or on dedicated metallic pads to improve the electrical contacts. Task II will extend the technique to confined three-dimensional volumes. For this purpose, dedicated structures have been fabricated, where fin arrays of dimensions compatible with SIMS have been electrically connected in parallel such that their electrical resistance can be measured. In both tasks, the candidate will focus on the MH measurements and simulations. Calculations will indeed also be needed to understand the impact of the contact geometry and of the confinement on the free carriers and currents inside the investigated structures.
This work will be done in the characterization group of imec disposing of a multitude of characterization techniques in support of this project. It will also be done in very close collaboration with the process engineers of imec and its industrial partners.

Type of project: Thesis or internship project or thesis combined with internship project with a minimum duration of 6 months

Degree: Master in Science and Master in Engineering majoring in Electrotechnics/Electrical Engineering, Physics

Responsible scientist(s):
For further information or for application, please contact Janusz Bogdanowicz (janusz.bogdanowicz@imec.be).

Composition measurements in advanced III-V nanostructures using Raman spectroscopy

One of the next steps in future-node semiconductor technology is the use of III-V compound semiconductors as a high-mobility channel material. The growth of these alloys on industry-standard Si wafers is challenging and may lead to the introduction of defects and compositional fluctuations. Accurate measurements of the latter are particularly difficult given the high surface-to-volume ratio of the structures and the large lattice mismatches with the substrate. In this topic, the use and optimization of micro-Raman spectroscopy is investigated for measuring the local composition in next-generation semiconductor architectures. Raman spectra for III-V materials are in general quite complex and the small dimensions of the region of interest further complicate the measurement. However, it was recently found that a nano-focusing phenomenon enables the confinement of the excitation light inside the structures, leading to considerable enhancement of the Raman response. The internship will involve experimental work on state-of-the-art transistor structures combined with the development of a thorough understanding of the III-V Raman coupled modes. The resulting compositional measurements will be correlated with complementary metrology but the experimental work focuses on the Raman spectroscopy. The student will learn to work with a micro-Raman system using different laser wavelengths. A strong physics background is required. The student will be trained in working with a Raman system and characterize advanced semiconductor device structures. He/she will be part of the materials and component analysis (MCA) department.

Type of project: Internship project with a minimum duration of 6 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Materials Engineering, Physics, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Thomas Nuytten (Thomas.nuytten@imec.be).

Transmission electron microscopy: more than an image

Transmission electron microscopy (TEM) is an essential analysis technique for the development of advanced 3D semiconductor devices. It allows imaging of device structures with very high spatial resolution in different modes as well as chemical analysis of the local composition with sub-nanometer resolution. Interpretation of the images for metrology purposes is generally directly possible. However more advanced interpretation for extracting detailed (quantitative) materials properties requires further analysis of the images or spectra. E.g. strain analysis at defects and in devices can be done in several ways based on either high resolution lattice images or diffraction patterns, compositional analysis can be based on image contrasts or with X-ray or energy loss spectra, etc. For all these applications several software packages are available. The obtained results will be dependent on selected parameters and procedures in the software and may vary between different packages.
The work is focusing on the evaluation of different software packages for advanced interpretation of TEM results and application to different topics (strain, compositional analysis) making use of the vast database of TEM measurements of imec. The goal will be to determine best practices for several use cases and applications. It will require that the student obtains an excellent insight in the basics of electron beam/materials interactions and TEM image formation as well as of the materials properties that are investigated. Interest in materials and crystallography is therefore needed. The work is not focusing on software development or own use of the TEM instruments.

Ref : ImageEval ; http://en.wikipedia.org/wiki/Multislice ; http://tem-s3.nano.cnr.it/?page_id=2

Type of project: Internship project with a minimum duration of 6 months

Degree: Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Electrotechnics/Electrical Engineering, Materials Engineering, Physics, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Hugo Bender (hugo.bender@imec.be).

Metal deposition for future technology nodes

Traditionally, copper has been used for the metallization of semiconductor devices. For the industry to even further scale down such devices, to enable faster and more performing chips, the features are made smaller and smaller. At some point, material properties of copper are becoming problematic. Therefore, various alternative metals have been identified, such as ruthenium, rhodium, iridium, cobalt, and nickel. During the internship, we will focus on depositing the metal, study the nucleation and growth kinetics, and characterize the deposit with various techniques, such as electrochemical measurements, atomic force microscopy, scanning electron microscopy, transmission electron microscopy. The student will be executing the experiments and be involved in material characterization and data analysis.

Type of project: Internship or thesis project with a minimum duration of 3 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Materials Engineering, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Harold Philipsen (Harold.philipsen@imec.be).

Pt-group metal nanowires for advanced interconnects

Interconnect lines in today's integrated microelectronic circuits consist of Cu lines separated by a low-k insulating material. In future generations, the continuous dimensional scaling will bring the width of the interconnect lines to a few nm only. The usage of such very narrow lines will lead to several issues, which have to be addressed for Moore's law to continue for interconnects.
In nanometer thin metallic lines, surface and interface properties of the metal will become increasingly dominant over their bulk ones. This also means that the line resistance will be strongly influenced by surface or interface scattering. Cu is chosen in today's applications because of its very low bulk resistivity. However, when surface or interface effects dominate, Cu is not necessarily the best choice anymore and novel metallic materials are currently researched for improved resistivity in sub 10-nm narrow lines.
Recently, Pt-group metals (Ru, Ir, Rh) have shown great potential for interconnects with dimensions below 10 nm. A key part of the thesis will be the detailed study of scattering mechanisms in low-dimensional (2D, 1D) structures of Pt-group metal films. Pt-group metal nanowires will be fabricated in collaboration with the interconnect integration team at imec. Variable temperature resistance measurements, as well as magnetoresistance measurements, in combination with semi-classical resistivity modeling will be employed to determine the relative importance of phonon, scattering, surface scattering, as well as grain boundary scattering as a function of the critical dimensions of the nanostructures. Additional structural material characterization will be used to link the determined resistivity to the materials parameters, such as crystallinity or impurity concentrations.
Prospective students should be interested in a topic at the cross-over between nanotechnology, physics, materials science, and electrical engineering, both from an experimental, as well as a modeling point of view.

Type of project: Internship or thesis project with a minimum duration of 9 months

Degree: Master in Science and Master in Engineering majoring in Electrotechnics/Electrical Engineering, Materials Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Christoph Adelmann (adelmann@imec.be).

Simulations and design of spin wave based logic devices

Current semiconductor-based CMOS devices may reach their physical limits in the next decade. To be able to continue the scaling of the device dimensions, to improve the device performance, and to further lower the power per operation, the replacement of CMOS transistors by novel types of devices may become necessary. Currently, a number of such technologies and concepts are being considered, including devices based on the interference of spin waves. Basic building blocks of such devices are ferromagnetic waveguides as well as transducers between the electrical (microwave) and the magnetic (spin wave domain). Experimental spin wave devices that are currently studied typically use co-planar microwave waveguides as transducers that generate and detect spin waves using inductive coupling. This enables all-electrical microwave measurements of basic spin wave devices [1].
At present, spin wave based computing should be considered a concept at TRL 2. While basic physical principles of spin waves are known for several decades, advancing the TRL of spin wave devices will require to optimize the waveguides and transducers, e.g. in terms of energy efficiency and output signal magnitude. Currently, simulations of spin wave based devices are carried out using micromagnetic simulations and focus strongly on the magnetic waveguide without including a detailed quantitative description of the transducer behavior. This imposes strong limitations on the simulation and design of basic spin wave devices, e.g. like the ones studied in [1]. Therefore, it is of great interest to develop simulations and design methods for spin wave based devices that can include spin wave transducers and the resulting coupling efficiency, as well as the microwave periphery circuitry.
The propagation of the spin waves is described by the nonlinear Landau-Lifshitz-Gilbert (LLG) equation whereas the inductive coupling to a microwave electromagnetic field is described by Maxwell's equations. Currently, the simultaneous solution of LLG and Maxwell's equations for realistic devices is still very challenging (in part due to different length scales involved) and Maxwell's equations are typically neglected in micromagnetic spin wave simulations. Moreover, due to the nonlinear properties of LLG, such simulations are limited to the time domain. However, experimental studies are typically carried out in the frequency domain [1]. In this thesis, we therefore propose to use a linear approximation of LLG in combination with Maxwell's equations to simulate and design spin wave devices including microwave waveguide based transducers as well as periphery circuits. Such simulations are analogous to simulations of ferrite based devices employing ferromagnetic resonance that have been performed using standard microwave simulation software packages. Such simulation methods will be then employed to design and optimize spin wave devices and transducers with the aim to improve the coupling between electrical and spin wave domains as well as to minimize microwave losses in the periphery circuitry. The simulations will be performed in close collaboration with experimentalists and device physicists with the ultimate goal to validate the simulations by experimental realizations and measurements of the designed devices.
Prospective students should be interesting in modeling advanced logic devices at the interface between electrical engineering and physics. Some background in microwave electronics and/or magnetic materials is a plus.

[1] F. Ciubotaru, T. Devolder, M. Manfrini, C. Adelmann, and I.P. Radu, Applied Physics Letters 109, 12403 (2016).

Type of project: Internship or thesis project or combination of both with a minimum duration of 6 months

Degree: Master majoring in Electrotechnics/Electrical Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Christoph Adelmann (adelmann@imec.be), Florin Ciubotaru (Florin.Ciubotaru@imec.be) and Xiao Sun (Xiao.Sun@imec.be).

Modeling of magnetoelectric coupling for advanced spintronic applications

Spintronics is a novel field of electronics that uses the spin of electrons or the magnetization of thin films instead of charge in memory or logic computation devices. A key issue of spintronics is the energy-efficient control of the magnetization in such devices. Current device concepts are often based on the control of the magnetization by currents, for example via generated magnetic fields or recently discovered effects, such as spin-transfer torque or spin-orbit torque. However, such techniques are typically not very energy-efficient and it would be very desirable to control the magnetization by electric fields instead. In principle, this can be done by the magnetoelectric effect, which couples electric fields to the magnetization. This effect is currently strongly considered to be included in future generations of low-power spintronic devices.
Magnetoelectric effects naturally occur in multiferroic materials but much stronger strain-induced magnetoelectric coupling can be observed in composite materials consisting of piezoelectric and magnetostrictive materials. Although the effect has been described already several decades ago, the application in spintronic devices requires a detailed understanding of the effects of the geometry (e.g. the relative directions of the electric field and the magnetization) as well as thermal fluctuations on the magnetization dynamics. Remarkably, this has not been studied in detail before and is currently a major roadblock for the design and development of spintronic devices that use the magnetoelectric effect. In this thesis, the student will develop analytical models for the magnetoelectric coupling in different geometries and different material systems and study these further using micromagnetic simulations both without and with the effect of thermal fluctuations. An important parameter will be the magnetocrystalline anisotropy of the magnet. The goal of the thesis is to develop efficient strategies to excite, control, and detect magnetization dynamics (including both magnetic switching as well as spin waves) by the magnetoelectric effect and transfer them to a magnetic waveguide. The work will be in close collaboration with experimentalists working on integration of magnetoelectrics into spintronic devices for beyond CMOS logic.

Type of project: Thesis project

Degree: Master in Science majoring in Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Christoph Adelmann (adelmann@imec.be), Florin Ciubotaru (Florin.Ciubotaru@imec.be) and Adrien Vaysset (adrien.vaysset@imec.be).

Physical mechanisms for the detection of magnetization textures for novel spintronic devices

With the recent advances in the field of spintronics, magnetization textures such as domain walls, skyrmions and spin-waves have become promising candidates to substitute ``ordinary" electrons as information carriers in next-generation electronic devices. Information carriers need to be manipulated efficiently in order for spintronic devices to function properly. Therefore, efficient creation, annihilation and detection of those carriers is a crucial aspect of the performance of such devices.
The aim of the current thesis is to explore schemes that can be used for efficient detection of magnetization textures. These textures can range from simple ones, e.g. 1D Domain wall, to more complex such as a 2D skyrmion texture. Moreover, they can also vary in time as in the case of spin-waves. Current research in the group has focused on interaction of static magnetic textures with strong spin-orbit coupling materials. In such materials, spin and momentum are not two independent degrees of freedom, but are coupled to each other. As a result, any effect on the spin can instantly be translated to momentum scattering. It would be helpful therefore to explore additional materials that can be used for magnetic texture detection and compare the results with those of the current study. The investigation can start from simple models that contain only the most important mechanisms and gradually build-up to include more realistic details. If time permits it more complex magnetization structures such as spin-waves can also be investigated.
Background knowledge in the field of quantum mechanics, solid state physics and magnetism is preferred.

Type of project: Thesis project

Degree: Master in Science and Master in Engineering majoring in Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Dimitrios Andrikopoulos (dimitrios.andrikopoulos@imec.be) and Bart Soree (bart.soree@imec.be).

Area selective deposition – bottom up strategies for patterning

Over the last decades, the dimensions of micro-electronic devices have been continuously scaled down, leading to exponential gains in computational power and reduced production cost. However, as the device dimensions are shrinking further, this scaling brings significant challenges to photolithography, which becomes increasingly complex and expensive. In addition to the issue of resolution, the accurate pattern placement is a major concern. Therefore, the combination of the conventional "top-down" patterning techniques with alternative "bottom up" strategies for patterning is necessary. Examples include self-aligned multiple patterning, directed self-assembly and area selective deposition. In area selective deposition, differences in surface reactivity are exploited to deposit material only according to certain predefined patterns, while other patterns on the same substrate remain unaffected. This selectivity can be achieved by processes that are based on specific precursor reactions in chemical vapor deposition (CVD) and atomic layer deposition (ALD). Today, practical applications of area selective deposition in patterning are still limited because area selective deposition is demonstrated only for few material combinations and the obtained selectivity is rarely sufficient. A better understanding on the role of the precursor of ALD and CVD processes is essential to expand the material combinations accessible by area selective deposition as well as to improve selectivity. The general aim of this internship project is to generate insight in suitable precursor chemistries for area selective ALD and CVD processes for patterning applications. The impact of the precursor, co-reagent and process conditions and how these affect selectivity needs to be better understood, so that the process window for selective deposition can be broadened to enable applications in patterning. Both inherent selectivity and surface treatments that increase selectivity will be investigated. The area selective deposition approaches will be investigated on pre-patterned substrates with patterns of nm-scale dimensions. We leverage Imec's 300mm production line and advanced node technologies to gain access to patterned structures with dimensions down to tens of nanometers in order to do industrially relevant research of area selective deposition for patterning applications. For different precursors, we will assess the selectivity window by investigating the nucleation mechanisms on the "growth" and "no growth" surfaces. The latter is of importance as insight in the mechanisms for selectivity loss can be used to design processes with improved selectivity.

Type of project: Internship project with a duration of 4 to 6 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Materials Engineering, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Annelies Delabie (Annelies.delabie@imec.be).

Impact of higher order precursors on epitaxial growth of SiGeSn alloys

Down scaling of MOS devices has been major impetus of semiconductor industry. The concept of "More Moore" becomes physically (tunneling and leakage currents), material wise (requirement for highly doped materials), thermally (low thermal budget and less power consumption) and economically (cost reduction) challenging for technology nodes beyond 22nm. New device concepts require cutting edge material research to achieve desired performance levels. SiGeSn is one such material which has ability to behave as direct band gap and offers to independently tune band gap & strain levels (lattice constants). SiGeSn is probable candidate for both logic applications S/D areas of n(p)FETs and silicon based photonics (e.g. strained Ge grown on top of SiGeSn SRB (Strain Relaxed Buffer) to confine carriers for improved emission characteristics).

However fabrication of SiGeSn alloys is extremely challenging task due to high risk of Sn precipitation because of its limited solubility. This sets the requirement for ultra-low thermal budgets and to explore the non-conventional precursors to deposit complex SiGeSn compounds. It is of upmost importance to understand the chemistry for higher order precursors and the impact of growth conditions on material properties. Insight into the type of defects incorporated during epitaxial growth and their interaction with co-dopants is important to understand dopant activation. In-situ boron or phosphorous doping of Ge with other isovalent atoms (Si, Sn) might help to achieve high dopant activation in as grown layers.
Using Chemical Vapor Deposition the candidate will assess how the choice of growth precursors affects the material properties. Correlation between the defect formation, strain state and its impact on material properties will be studied. To understand electronic band structure of heterojunctions, we will calculate how the electronic band gap varies as function of composition and strain (e.g. strained Ge1-xSnx/ SixGe1-x-ySny strain relaxed buffers). The calculated values of band gap using theoretical modelling will be compared with measured values. As different Si and Sn compositions in SiGeSn epitaxial layers can be tuned to obtain the same lattice constant. The impact of different compositions with the same lattice constant on active doping levels for both the n and p-type layers will also be studied. In the end, candidate is expected to summarize all the research findings in thesis report.

Type of work: 50% experimental, 15% theoretical study, 15% literature, 20% thesis report

Type of project: Thesis project with a duration of 6 to 9 months

Degree: Master in Science majoring in Electrotechnics/Electrical, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Roger Loo (Roger.Loo@imec.be) and Anurag Vohra (Anurag.Vohra@imec.be).

Design and characterization of reliable Physically Unclonable Functions in CMOS

For modern hardware security applications, a physically unclonable function (PUF) is a building block with emerging importance, which enables chip level secret key generation, counterfeit identification, IP protection and entity authentication. A conventional PUF implemented in CMOS technologies generates and stores an unique data pattern resulted from the intrinsic process variations, which is random within the same chip and between chips. The readout procedure for PUF data is somehow vulnerable to noise due to the low magnitude of the variations, which introduces bit instability. Moreover, the aging of devices can reduce the mismatch between cells which will also degrade the stability of PUFs.
In order to tackle the instability, the understanding of reliability physics has a growing importance in the PUF designs. The reason is not limited to reduce the effect of aging, but also to develop special aging methods to enhance PUF performance. Several works have proposed the idea of using bias-temperature instability (BTI) and hot-carrier injection (HCI) degradation mechanism to eliminate bit instability. A recent work proposed by IMEC-DRE and COSIC utilizes the position of oxide breakdown in CMOS transistors (concept as Fig.1), has been proven to have even better performance and is more feasible in real applications. The candidate of this thesis work will involve in this ongoing project, working together with our reliability and security researchers to gain knowledge for a reliable PUF design.
This thesis work would focus on electrical characterization of existing PUF test structures and devices in modern CMOS technologies, to assess the performance and feasibility of employing oxide breakdown or other kinds of degradation mechanisms. The candidate may also contribute in a real circuit design on PUF using a commercial CMOS process, which requires a basic knowledge on electric circuits. The other requirement for this thesis is knowledge on semiconductors devices and basic statistics. The candidate need to learn cryptography and hardware security during this work, and a basic skill of a programming language (e.g. Python) is strongly recommended.

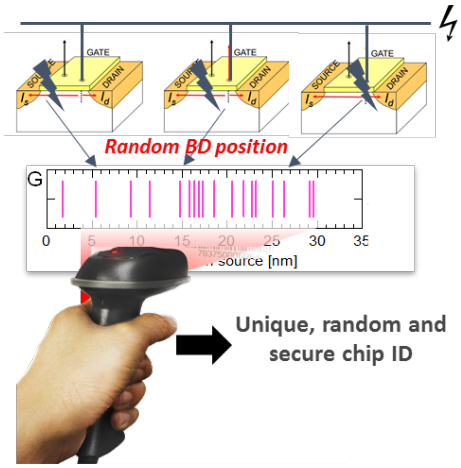


Fig. 1. Concept of PUF using breakdown position

Type of project: Thesis project

Degree: Master in Engineering majoring in Electrotechnics/Electrical Engineering, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Kent Chuang (Kai.Hsin.Chuang@imec.be) and Erik Bury (Erik.Bury@imec.be).

Spin wave devices for beyond CMOS applications

Current semiconductor-based CMOS devices may reach their physical limits in the next decade. To be able to continue the scaling of the device dimensions, to improve their performance, and to further lower the energy cost per operation might require the introduction of new and disruptive technologies. Spintronic devices based on spin waves (magnons) are promising alternatives to CMOS with high potential for significant power and area reduction per computing throughput. However, to be competitive with actual CMOS technology the spin wave devices need to tackle waves with wavelengths below 100 nm and a miniaturization down to the nanoscale. In this regime, the spin waves are increasingly driven by the exchange interaction. The study of such exchange spin waves is experimentally very challenging since their excitation requires the generation of oscillating magnetic fields comparable to the wavelength of the spin-wave in the nanometer range. For this reason, conventional excitation structures using microwave waveguides in the micrometer range cannot be used efficiently for the excitation of spin waves in the exchange regime. To approach the exchange regime novel miniaturized nanoscopic structures are currently designed. Within this thesis, the student will fabricate spin-wave devices based on different magnetic materials, from micro- down to the nanoscale and will contribute to their characterization in the microwave frequency range leading to important properties as spin wave dispersion relation, their damping and their propagation characteristics in the linear and non-linear regimes. The results will be an important step to understand the emission, the routing and the combination/interference of spin waves to continue the assessment of the concept devices as alternatives or complements to CMOS transistors in future technology nodes. The experimental work will be performed in close collaboration with modeling activities (materials, devices, circuits) in the spintronics group at imec. The student should have a strong interest in nanofabrication in a cleanroom environment as well as in leading edge research topics on magnetism and magnetic materials.

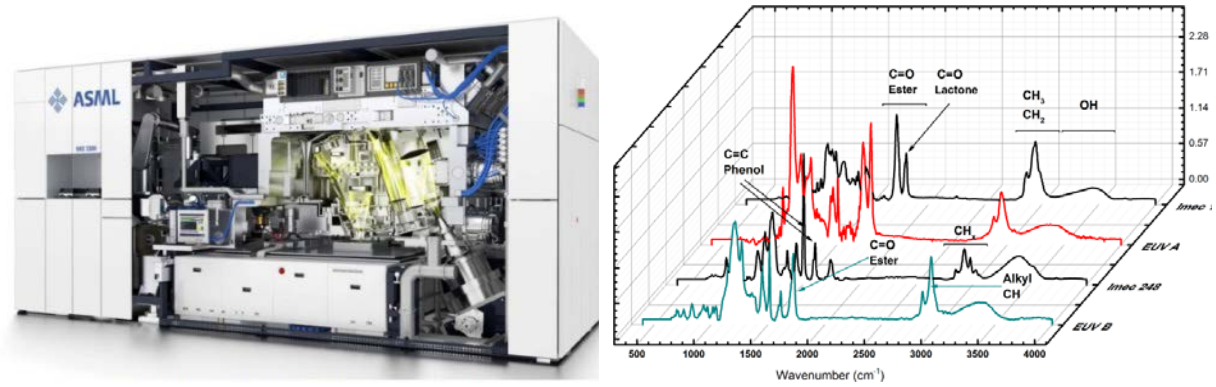
Type of project: Thesis or internship project or combination of both with a minimum duration of 6 months

Degree: Master in Science and Master in Engineering majoring in Electrotechnics/Electrical Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Florin Ciubotaru (Florin.Ciubotaru@imec.be), Christoph Adelmann (Christoph.Adelmann@imec.be) and Iuliana Radu (Iuliana.Radu@imec.be).

Characterization of photoresist for EUV lithography

Extreme ultraviolet lithography (EUVL) is the candidate for scaling down of semiconductor devices beyond the 10 nm technology node.
Using projection lithography at a wavelength of 13.5nm (soft X-ray), a light pattern is transformed into a chemical pattern in the photoresist. This functional material needs to be engineered such that 91.6eV photons induce a change of dissolution properties. Current photoresists are composed of a blend of specific polymer, photo-acid generator and quencher molecules. In order to have a more fundamental understanding of the mechanism of patterning, chemical studies need to be performed. The transformation can be studied by Fourier Transform InfraRed spectroscopy (FTIR) while the dissolution properties of a photoresist can be measured by the dissolution rate monitor (DRM) tool. Further techniques are in development to measure the acid yield in a photoresist as a function of exposure to light.
In the frame of this internship study, the student will characterize different photoresists to contribute to the understanding of their patterning mechanism under EUV light.
The student will be involved in the preparation of multiple samples under different process conditions and he will characterize the photoresist by using different techniques. The student will collect and interpret FTIR spectrum and measure dissolution rate using DRM. Further, he will help in the setup of the acid yield measurement protocol. The goal is to link the different results obtained in order to identify key material parameters (i.e. activation energy, yield) for the chemical reactions involved.
The student will be guided in his tasks by experienced users of the tools, and his results will be used to better understand the chemistry of the investigated photoresists, in collaboration with the commercial material suppliers.
To accomplish his task, the student has to have a background in polymer science, photochemistry and FTIR spectroscopy. Experience with FTIR spectra collection is a plus. Good knowledge of Excel is required.



Figures: Left, NXE scanner available at imec [1]. Right, FTIR spectrum of EUV photoresists [2]

[1] https://www.semiwiki.com/forum/content/4709-extending-euv-lithography.html
[2] De Schepper P, Hansen T, Altamirano-Sanchez E, et al; Line edge and width roughness smoothing by plasma treatment. J. Micro/Nanolith. MEMS MOEMS. 0001;13(2):023006. doi:10.1117/1.JMM.13.2.023006.

Type of project: Internship project

Degree: Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Materials Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Danilo de Simone (Danilo.DeSimone@imec.be), Geert Vandenberghe (Geert.Vandenberghe@imec.be) and Stefan De Gendt (Stefan.DeGendt@imec.be).

Digital design of flexible deep learning kernels

During the past year, the community has witnessed the advent of machine learning as one of the driving workloads of accelerator architectures. Deep learning (with all the associated flavors of neural networks) appears to be a valid force behind the research and development of computing accelerators, with non-volatile memories (NVMs) searching for a good place in the accelerator memory hierarchy. The current Thesis/Internship project will start from a well-defined deep learning architecture and will contribute to the RTL coding of many useful hardware blocks. We are looking for strong RTL coders than can maintain and develop production-level implementations, with language of preference being Verilog (however knowledge of VHDL will be considered equivalent). The student will have the chance to interact with the hardware design and algorithmic specification teams, so as to assist them in developing modules of a flexible and NVM-compatible deep learning architecture. Apart from RTL design and verification (tool of preference: Modelsim), the student will delve into the logic synthesis of the designed modules (tool of preference: Synopsys Design Compiler). The project can also be extended with the placement and routing of the digital design modules (tool of preference: Cadence Innovus). Understandably, proficient knowledge of the aforementioned tools cannot be expected by a student at a level of a Master Thesis. However, a motivated student with good knowledge of RTL design, fundamental grasp of computer architecture and basic knowledge of scripting languages (e.g. Bash, Python, Perl) will have the chance to familiarize with the above tool chain by interacting with the in-house team. As a result, apart from required coding competencies (Verilog, VHDL), the student is expected to deliver punctual status updates and be diligent in reporting progress and results. Basic knowledge of NVM technology fundamentals will be considered a strong plus.
Finally, the student is expected to have excellent communication skills and be independent in covering any knowledge gaps that may come up by interacting actively with the research ecosystem around them.

Type of project: Thesis with internship project with a minimum duration of 6 months

Degree: Master majoring in Electrotechnics/Electrical Engineering, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Praveen Raghavan (Praveen.Raghavan@imec.be), Dimitrios Rodopoulos (Dimitrios.Rodopoulos@imec.be) and Arindam Mallik (Arindam.Mallik@imec.be).

Algorithmic formulation of Hierarchical Temporal Memories

Hierarchical Temporal Memories (HTMs) have received significant attention from the machine learning community as valid tools for the prediction of time series and temporal anomalies found therein. Following the exponential growth of data produced by various human activities, it is considered very urgent to deploy such machine learning kernels at increased energy efficiency and near-real-time performance. A variety of memory technologies is explored, as a result, to aid and enable the semiconductor integration of HTMs. Among them, non-volatile memory (NVM) technologies appear to be promising candidates. The current Thesis/Internship project will look into an existing HTM implementation and will extend/enhance it towards increased functionality and testability. We are looking for strong coders than can maintain and develop production level implementations, with languages of preference being Python and C. The student will have the chance to interact with the algorithm development team and assist them in developing and testing HTM concepts on a mature software platform. In parallel with software-based testing, HTM concepts will be tried on diced and packaged NVM chips, so as to demonstrate their suitability with memristive technologies. To that end, a portion of this work will involve the coding of Python interfaces to NVM boards, in order to enable faster and more reliable/realistic HTM experiments. Apart from required coding competencies (Python, C), the student is expected to deliver punctual status updates and be diligent in reporting progress and

results. Basic knowledge of NVM technology fundamentals (e.g. resistive RAM) and basic computer architecture will be considered a strong plus. Finally, the student is expected to have excellent communication skills and be independent in covering any knowledge gaps that they may come across by interacting actively with the research ecosystem around them.

Type of project: Thesis with internship project with a minimum duration of 6 months

Degree: Master majoring in Electrotechnics/Electrical Engineering, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Praveen Raghavan (Praveen.Raghavan@imec.be), Dimitrios Rodopoulos (Dimitrios.Rodopoulos@imec.be) and Robin Degraeve (Robin.Degraeve@imec.be).

Characterization and understanding of semiconductor materials for advanced CMOS

The integration of semiconductor materials such as Germanium (Ge) and III-V compounds (InGaAs, InAlAs) into a 3D device architecture (FinFET, nanowire-FET) appears indispensable to facilitate CMOS scaling beyond the 7nm technology node. While 3D device architectures aid in improving the electrostatics, thereby limiting the overall power dissipation, the aforementioned semiconductors with their significantly lower effective masses boost the drive current and hence performance of future transistors.
However, the 3D integration of new materials combined with the ever decreasing device dimensions imposes many challenges on device fabrication and understanding of the relevant material properties. For this reason we are exploring a number of materials characterization techniques to assess the dimensions, material quality (e.g. crystalline defects), composition (e.g. Indium content in InGaAs) and degree of strain and stress in 3D fin structures.
To address these metrology challenges, we are continuously looking for knowledgeable and motivated students with a background in semiconductor physics and/or technology or material science. Depending on the student's expertise and interests, the specific internship/thesis subject will be selected from the following research topics:

- Study of extended crystalline defects (dislocations, stacking faults) using electron channeling experiments
- Investigation of semiconductor material quality using time-resolved photoluminescence
- Analysis of strain and composition in fins and nanowires using high-resolution XRD
- Simulation of mechanical strain and stress distributions in nanometer scale 3D structures using Comsol
- Dimensional metrology using X-ray diffraction and X-ray scattering

In the initial phase the student will receive an in-depth training on the respective hard- and software tools. The student will then further develop and apply the aforementioned concepts to study different materials and structures in close collaboration with metrology researchers as well as process/integration engineers. The supervisor will guide the candidate to ensure the scientific character of the internship and/or thesis.

Type of project: Thesis or internship project or combination of both with a minimum duration of 6 months

Degree: Master in Science and Master in Engineering majoring in Electrotechnics/Electrical Engineering, Nanoscience & Nanotechnology, Materials Engineering, Physics

Responsible scientist(s):
For further information or for application, please contact Andreas Schulze (Andreas.Schulze@imec.be).

Optical characterization of 2D semiconductors

Recently, there is a growing interest in the family of two-dimensional (2D) transition-metal dichalcogenide (TMD) semiconductors MX2 (M stands for Mo, W or Sn and X stands for S, Se or Te). The most extensively studied member of this family is MoS2. The latter is an indirect bandgap material in its bulk form, however, becomes a direct bandgap semiconductor (Eg=1.88eV) when thinned to a monolayer. Such a wide bandgap and the structural similarity with graphene makes the material an interesting candidate for potential applications in logic electronics. The most common fabrication procedure for single to few-layer MX2 is mechanical exfoliation ("scotch tape method") from high-quality natural bulk MX2 crystals. However, exfoliation techniques suffer from small flake sizes and yield limitations which prevents the technique from being adopted for large scale applications. For this reason, imec is currently exploring various methods for growing high-quality large-area few-layer MX2. In order to support the development of such processes, adequate characterization tools capable of analyzing e.g. the layer thickness, the crystalline orientation and the layer stacking need to be provided, too. This becomes particularly challenging due to the limited volume available for the analysis as well as the demand for non-destructive techniques with mapping capabilities.
The goal of this internship is to explore and understand the possibilities of spectrocopic and time-resolved photoluminescence at room as well as low temperature to study the optical transitions as well as the crystalline structure of various TMDs. The measurements will be correlated with more established techniques such as Raman spectroscopy, AFM and TEM.

Type of work: 20% literature study, 40% experimental work, 40% analyzing, modeling and understanding

Type of project: Thesis or internship project or combination of both with a minimum duration of 6 months

Degree: Master in Science and Master in Engineering majoring in Electrotechnics/Electrical Engineering, Nanoscience & Nanotechnology, Materials Engineering, Physics

Responsible scientist(s):
For further information or for application, please contact Andreas Schulze (Andreas.Schulze@imec.be).

Magnetic domain wall injector

Magnetic domains are commonly used in memory applications such as hard-disk drives and Magnetic Random Access Memory (MRAM). The intrinsic non-volatility of magnetic materials makes them perfect for long-term storage of information. However, they can also be used to compute logic operations. For example, in domain wall logic, magnetic domains move along a strip to propagate information. The logic levels "0" and "1" are represented by the magnetic orientation. So far, the spintronics community has focused on the physical mechanisms that govern domain wall motion, allowing continual increase in domain wall speed. However, almost all the studies relied on a basic method to inject domain wall. This method, which consists in generating a magnetic field via a current in a wire, is very unpractical and inefficient for real-world applications. A new way to efficiently inject domain walls in a nanowire was recently found at imec, thanks to micromagnetic simulations. The goal of this master thesis is to build for the first time this domain wall injector. It will be a major progress for applications such as domain wall logic and racetrack memory. The candidate will design and fabricate Hall bar devices at imec's LAB clean room and characterize their magnetic and electrical properties. A strong background in solid state physics is desired. This topic is very hands-on and the candidate is expected to have a clear motivation to work in the clean room.

Type of project: Thesis project

Degree: Master in Science and Master in Engineering majoring in Nanoscience & Nanotechnology, Materials Engineering, Physics

Responsible scientist(s):
For further information or for application, please contact Adrien Vaysset (adrien.vaysset@imec.be) and Mauricio Manfrini (mauricio.manfrini@imec.be).

Spintronic memristor

Magnetic domains are commonly used in hard-disk drives and Magnetic Random Access Memory (MRAM) to store information. When these domains are inside a magnetic strip, they can be moved by several means, such as Spin Transfer Torque (STT) or Spin-Orbit Torques (SOT). Several applications using domain wall (DW) motion have been considered, in particular for logic and memory. But DW can also be used for neuromorphic computing, which combines both logic and memory. In this case, the DW motion induces a change in resistance, thus leading to a new device, called "memristor". This is the key component to build large-scale neuromorphic circuits that will enable efficient and low-power implementation of machine learning algorithms. The goal of this thesis is to build DW-based memristor devices and to propose innovative solutions for the controllability of the domain wall. The candidate will design and fabricate Hall bar devices at imec's LAB clean room and characterize their magnetic and electric properties. A strong background in solid state physics is desired. This topic is very hands-on and the candidate is expected to have a clear motivation to work in the clean room.

Type of project: Thesis project

Degree: Master in Science and Master in Engineering majoring in Nanoscience & Nanotechnology, Materials Engineering, Physics

Responsible scientist(s):
For further information or for application, please contact Adrien Vaysset (adrien.vaysset@imec.be) and Mauricio Manfrini (mauricio.manfrini@imec.be).

Surface and interface engineering of 2D semiconductors and their applications for electronics

Meeting the technology requirements for the next-generation semiconductor devices represents a formidable challenge which will require new device architectures and novel materials. In this context, layered materials like transition metal dichalcogenides (MoS2, WSe2, etc.) are emerging as potential post-Si semiconductors, especially as scaling progress towards ultrathin body devices. 2D TMDs consist of molecular layers stacked together by weak van der Waals interactions. This characteristic structural feature enables the synthesis of ultra-thin films with atomic scale smoothness and no dangling bonds thus providing superior electrostatic control of the channel and reducing the effects of surface roughness scattering. Beside the synthesis of high quality 2D materials, doping techniques and contact resistance are other key areas which require significant experimental work to meet the future technological challenges for high performance logic devices. Given their ultra-thin body nature, the electronic properties of TMDs are more susceptible to interactions with the surrounding environment. Therefore, interface engineering represents a logical route to tune and boost the electrical performance of TMD-based devices. The broad objective of this master's thesis work is to gain atomic-scale understanding of 2D TMDs and investigate interface related properties. Novel interface/phase engineering approaches will be explored and optimized with the main goal to improve device performance and materials efficiency.
The work will include:

- Physical characterization of 2D TMDs (Raman, XPS, AFM)
- Material functionalization/engineering
- Device fabrication in a clean-room environment
- Device characterization
- Data analysis

Type of project: Thesis project

Degree: Master in Engineering majoring in Bioscience

Responsible scientist(s):
For further information or for application, please contact Daniele Chiappe (Daniele.Chiappe@imec.be) and Cedric Huyghebaert (Cedric.Huyghebaert@imec.be).

Emergent electromagnetic fields and Topological Hall Effect for magnetic skyrmions

In metallic magnets, conduction electrons that are subjected to non-collinear or non-coplanar magnetization or spin textures such as domain walls or skyrmions give rise to an emergent electromagnetic field. This is due to the coupling between the intrinsic spin of the conduction electrons and non-trivial spin or magnetization texture. The Lorentz force that arises from the emergent magnetic field gives rise to the topological Hall effect. In literature, there exist experimental reports of the topological Hall effect in MnSi, FeGe and MnGe. The Skyrmion induced topological Hall effect could be a possible route for the electrical detection of skyrmions which is required for making them useful for memory or logic. Efficient electrical detection is a key aspect for next-generation skyrmion-based devices.
The aim of the current thesis is to model the physical mechanisms that give rise to the Hall effect induced by topological-protected structures. In this way, a deeper understanding of the physics as well as the optimization that needs to be done for skyrmion-based devices will be gained.
The candidate should have sufficient background in quantum mechanics, solid state physics and magnetism. For any additional information, do not hesitate to contact the supervising scientists.

Type of project: Thesis project

Degree: Master in Science majoring in Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Bart Soree (Bart.soree@imec.be) and Dimitrios Andrikopoulos (Dimitrios.andrikopoulos@imec.be).

Defect reduction in directed self-assembly processes

With scaling of electronic devices, printing of the structures that are required to make them has become more and more complex and costly. For a few years, directed self-assembly (DSA) has been considered as a viable and low-cost alternative and complementary patterning option for keeping the down-scaling alive in the coming years, while ensuring an economic benefit to the silicon industry. DSA processes using block co-polymers to pattern uniform line-space patterns and arrays of holes with resolutions much smaller than the capability of the current lithographic nodes have been successfully demonstrated by various research/industrial groups around the globe. Several figures of merit have been identified and put forward as major checkpoints to assess the relevance of DSA processes for high-volume manufacturing environment; defectivity, roughness, placement accuracy, repeatability and robustness, cost of development and implementation being some of the important ones.
Your project will focus on one of the main factors that would make or break the show for DSA to be adopted by the IC manufacturers/production fabs – reducing the number of defects on the wafer after DSA and to be able to identify their root causes. Defects can be induced by various factors: non-ideal assembly (external and/or on-wafer) conditions, DSA material(s)-induced defects, non-DSA processes related defects (e.g. etch processes) and additionally in most cases, a cross-interaction of the above factors. One of the challenges in this study is to be able to identify/isolate the impact of the above factors on the different defect types we see after DSA. A routine part of this project will involve getting accustomed to advanced lithography tools (in our 300 mm production line environment), like immersion scanners/track clusters to define our process wafers and metrology tools like optical defect inspection, SEM-based defect review, CDSEM, optical scatterometers for characterizing and measuring defect densities of our processes and offline software packages for data analyses..

The main goal of your Masters' thesis/internship is to support and enable the defect reduction strategies of the DSA program at imec in the line-space and/or the contact hole DSA patterns, with inputs from both process improvements and running and optimizing the defect metrology. The ultimate aim of the study is to demonstrate the ability of the process to reproducibly deliver low defectivity on full 300 mm wafers. As you get familiar with the DSA process and defect inspection techniques, the focus of your study will shift more towards automated defect review/classification capabilities using a 300 mm in-line review SEM and a dedicated software platform that would reduce the need for manual defect classification, hence bringing down the data analysis duration by at least a factor 4. For this, you will leverage on the 14 nm half-pitch chemo-epitaxy DSA flow for line-space patterns developed in-house and on all the know-how about defect inspection/review strategies, both internally at imec and from external partners. A big part of your tasks will also include running the weekly defectivity monitor flow and analyzing the data from it, which acts as the baseline to assess the impact of the various defect reduction approaches we adopt.

Generic DSA literature:
1. H.S. Philip-Wong et al., Block Copolymer Directed Self-Assembly Enables Sublithographic Patterning for Device Fabrication, Proc. of SPIE Vol. 8323, 832303, 2012. doi: 10.1117/12.918312
2. W. Hinsberg et al., Self-Assembling Materials for Lithographic Patterning: Overview, Status and Moving Forward, Proc. of SPIE Vol. 7637 76370G, 2010. doi: 10.1117/12.852230

Project specific literature:
1. P. Delgadillo et al., Defect source analysis of directed self-assembly process (DSA of DSA), Proc. of SPIE Vol. 8680, 86800L, 2013. doi: 10.1117/12.2011674
2. P. Delgadillo et al., All track directed self-assembly of block copolymers: process flow and origin of defects, Proc. of SPIE Vol. 8323, 83230D, 2012. doi: 10.1117/12.916410
3. C. Bencher et al., Directed Self-Assembly Defectivity Assessment, Proc. of SPIE Vol. 8323, 83230N, 2012. doi: 10.1117/12.917993
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Type of project: Internship project

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Electrotechnics/Electrical Engineering, Materials Engineering, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Paulina Rincon (Paulina.RinconDelgadillo@imec.be) and Geert Vandenberghe (Geert.vandenberghe@imec.be).

LSTM architecture implementation using binarized neural network

An LSTM model (Long-short term memory) is a model designed to combat a common problem with RNNs (Recurrent Neural Networks) - it's difficult for them to learn long-term dependencies. LSTM seeks to solve the vanishing gradient problem. At its core, the LSTM layer is just a different way to compute the next hidden state, given a previous hidden state and a current state. They've been used successfully enough to become the current state of the art technique for using neural networks in NLP application. Recently there has been a lot of work involving reducing the size and computation cost of neural networks through quantization/binarization while maintaining the performance of the model at approximately the same level. For natural language processing or deep learning, it usually involves training language models of huge corpus and the training speed is slow as well. In this project, the student will look into applying the binarization of the LSTM cell with the goal of achieve a similar accuracy and boost in speed. The work would involve coming up with novel architecture to enable an efficient neuromorphic hardware implementation in terms of performance, power and area. The student has to explore, analyze and evaluate the benefits of neuromorphic hardware in using imec's in-house NVM technology. His/her work will involve cross-domain interaction from manufacturing technology to circuit design and system architecture.

Required background: Electrical and Computer Engineering with CMOS design background, preferable in the context of memory design. Previous experience with microarchitecture, MATLAB/PERL/C/C++ programming would help. Basic understanding of device architecture is preferred. The current thesis/internship project will start from a well-defined deep learning architecture. Basic knowledge of NVM technology fundamentals will be considered a strong plus. Finally, the student is expected to have excellent communication skills and be a good team worker as he has to interact with both device researchers and system designers.

Type of project: Internship or thesis project or combination of both with a duration of 3 to 6 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Computer Science, Electrotechnics/Electrical Engineering, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Praveen Raghavan (Praveen.Raghavan@imec.be), Arindam Mallik (Arindam.Mallik@imec.be) and Dimitrios Rodopoulos (Dimitrios.Rodopoulos@imec.be).

III-V gatestacks: Investigation into defect reduction

In order to meet the ever increasing demand for faster and more performant electronics, the semiconductor industry continuously strives towards transistor size reduction , known to many as Moore's law. This scaling constantly poses new challenges and – having entered the nanometer range - the silicon based technology is slowly reaching its fundamental limits. Therefore the semiconductor industry is looking towards alternative materials that could possibly replace silicon in future electronics. One of the most prominent candidates is the class of III-V materials, which consist of alloys between group III and V elements. These materials have already shown extraordinary electron mobilities (more than 10 times the mobility of silicon for InAs), can work at lower operating voltages (which reduces power consumption) and hold potential for future device architectures like gate-all-around field effect transistors (GAA-FETs) and tunneling FETs (TFETs).
Despite their high potential, production of high performance and reliable devices still remains an issue and hampers the large scale integration of III-V materials. Main challenges include chemical imperfections at the semiconductor-dielectric interface as well as defects (and charged sites) in the dielectric material itself. These defects cause electron trapping and scattering during device operation, resulting in a reduced performance and reliability.
The main focus of this project is to investigate the origin of these defects as well as possible treatments aimed at reducing the defect density. Given these defects originate from imperfections in the material (unsaturated bonds in the crystal/at the interface) most strategies will focus on a variety of chemical treatments aimed at saturating these bonds. These treatments include both liquid and gas phase processes, such as the use of sulfur compounds to passivate (S-terminate) the surface. Special attention should be paid to prevent any additional damages that might result in degradation of the material's properties and consequently degradation of the resulting device. This should improve device performance and reliability, bringing III-V materials one step closer to integration in future technology.
During this project the student will have the opportunity to perform research in imec's state-of-the-art cleanrooms and will have access to a wide variety of characterization techniques (both physical and electrical). Imec is generally considered as one of the world leaders in semiconductor research, and the student will have the opportunity to work together with many experts in their respective fields. The student will be able to make a contribution to advancing the field of III-V semiconductors.
All necessary trainings will be provided by imec. The specific focus of the project can be adjusted depending on the students interests and background. Ideally the student should be a motivated, eager to learn individual with an interest in semiconductors, surface/interface chemistry and material engineering.

Type of project: Internship project
This project is open to self-supported students only (no imec allowance will be provided).

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Materials Engineering, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Dieter Claes (dieter.claes@imec.be).

ESD reliability of high mobility finFET devices for ultimate CMOS

In the last decade, new processing features have been introduced into VLSI technology: source/drain stressors (90 nm node), high-k dielectrics and metal gate electrodes (45 nm node) and more recently, a new transistor architecture (finFET, multi-Gate FET or 3D-transistor) has been introduced. The next technology option to be possibly introduced into the FinFET device architecture, is the use of high-mobility (non-silicon) channel materials. For pFETs, (silicon)germanium-based devices are being considered due to their compatibility with the existing Si technology. For nFETs, III-V alloys such as InGaAs are being investigated. Note that the bulk hole mobility of Ge (1900 cm2/Vs) is significantly higher than that of Si (450 cm2/Vs). Similarly, the electron mobility in In0.53Ga0.47As (~12.000 cm2/Vs) is a lot higher than in Si (1400 cm2/Vs). A key reliability characteristic that needs to be investigated before any commercial product can be shipped, is it's ESD (Electrostatic discharge) reliability. An ESD event on an IC, is a discharge event where up to 10 A of current over a time span below 100 ns needs be able to flow through any 2 – pin combinations of that IC without destroying or wounding it. In order to coop with such an event, a pre-designed ESD current path must be layouted on the IC, using dedicated ESD clamps (voltage sensitive switched), which are off during normal operation and on during an ESD event. Such ESD clamps need to be evaluated in every new CMOS technology, and if needed to be optimized or altered. Based on excising test structures, destructive ESD measurements will be performed on various clamps and test structures. These measurements reveal the high current high voltage behavior which needs to be physically analyzed; also the failure signatures need to be understood. Once this is understood, ESD FinFET device layout optimization can be done, and ESD protection strategies developed. The multi-disciplinary work combines the use of ESD characterization tools, physical analysis of ESD device operation and the use of computer simulations to clarify the underlying physical operation. The work bridges the fields between advanced technology development, characterization tools, simulation and analog design. A student is sought, with a strong interest in semiconductor devices and a problem-solving mentality. The student will team up with imec's ESD experts, working with the latest experimental chip technology.

Type of project: Thesis project
This project is open to self-supported students only (no imec allowance will be provided).

Degree: Master in Engineering Technology majoring in Electrotechnics/Electrical Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Geert Hellings (geert.hellings@imec.be) and Shih-Hung Chen (Shih-Hung.Chen@imec.be).

Assessment of the FeFET capabilities as synaptic node in neuromorphic computation

As predicted by Moore's law , the computing power increased exponentially over the few past decades, propelled by the scaling of the mainstream CMOS technology . The number of transistors integrated on a chip has already penetrated the billion limit . While the number of components on the chip still remains about 2 orders of magnitude below the number of neurons in the human brain, the power consumption, by now exceeding 100W, has already surpassed that of the biological brain realm. This mismatch in the complexity-power pair is amplified when considering contemporary computing systems, traditionally based on the von Neumann architecture model . This assumes separate processing unit and memory, connected to each other, and being programmed to execute computational tasks in a serial manner, which largely affects the computational efficiency, especially in data-intensive applications. To achieve a higher computing complexity, which, on a longer term, aims at mimicking the way the

human brain works, a paradigm shift is needed. The promise of neuromorphic computing lasts in its massive parallelism, realized by strongly interconnecting many simple neuron processing units through artificial synapses, so as to emulate biological brain behaviour and be able to solve complex, data-intensive tasks, with limited power consumption. Crucial to the success of this approach is the need for strong interconnectivity, which, in turn, requires availability of dense and extremely scalable artificial synapses that must have the ability to adapt and respond in an analogous manner, just like their biological counterpart.
A step forward has been taken with the emergence of new nonvolatile memory technologies that use resistance, spin, or polarization to store information, opening a path for densely interconnected memory arrays, which can be used for non-von Neumann computing architectures.
Ferroelectric memory, although known for a long time, has recently seen a huge technological advance, enabled by the discovery of the ferroelectricity in HfO2, which opened a path for CMOS compatible technology integration. The scope of this work is to assess the suitability of a Ferroelectric Field-Effect Transistor (FeFET) as a synaptic component in neuromorphic computing systems. To this end, samples processed in imec's Pline will be used, and characterized electrically, using state-of-the-art instrumentation and a methodology that will focus on the use of the device as a synaptic element with binary or multilevel operation, identification of the operating window, assessment of the different trade-offs between performance and reliability. Aspects such as scaling impact on the synaptic device attributes will be also a point of interest. Depending on the format/duration of the work, the device will be benchmarked against other devices based on different mechanisms, considering offline or online training strategies and using a suitable simulation environment and test problems.

Type of work: 20% literature, 50% electrical characterization, 30% data analysis

Type of project: Thesis project with minimum duration of 4 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Electrotechnics/Electrical Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Bogdan Govoreanu (govorean@imec.be).

Doppler profilometry

Laser Doppler Vibrometry (LDV) is an optical technique which is used to measure out-of-plane displacements of objects as function of time with accuracy of sub-nanometers by measuring Doppler frequency shift of the signal reflecting from moving (dynamic) objects (for example MEMS).
The main objective of the student will be to explore if this technique can be applied to measure shape (profile) of a static surface. The basic principle of the "Dynamic Profilometry" technique has been developed at IMEC and the preliminary experiments have already been performed. However, more thorough and systematic study needs to be executed to further explore the applicability of the proposed method.
The student has to be familiar with electrical measurement techniques. Knowledge of optical technics and automation control (piezo-electric / electro-mechanical actuators and motors) will be appreciated.
During the work the student will:

- Learn laser Doppler vibrometry technique
- Perform automatization of electrical and optical measurements (programming in labview or Python)
- Build the prototype with electrically actuating mirrors or sample holders
- Perform visibility study to explore applicability and limitations of the technique
- Write and present technical reports

Type of project: Internship or thesis project or combination of both

Degree: Master in Engineering majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Vladimir Cherman (Vladimir.Cherman@imec.be) and Jeroen De Coster (Jeroen.DeCoster@imec.be).

Comparison of Strained SiGe epitaxial growth on Si vs SiGe SRBs in view of advanced MOS devices

Current down scaling of MOS devices goes together with modifications of the transistor device geometry, the implementation of new materials, and the introduction of new device concepts. Planar devices have been replaced by FinFET structures and new designs such as Gate All Around FETs are being considered to tackle future scaling issues. In parallel, Si has successfully been replaced by strained SiGe in high mobility channels as well as for the implementation of Source/Drain stressors. Compressively strained SiGe has beneficial material properties, especially the higher hole mobility makes it attractive for pMOS devices. In the same way, tensile strained Si enables to boost electron mobility. The combination of tensile strained Si and compressively strained SiGe sets the need to use so-called Strain Relaxed Buffers (SRBs) on top of which the active layers are grown (tensile strained Si for nMOS and compressive strained SiGe for pMOS). In this approach the Ge content in the SiGe channel is increased in comparison to the original concept of strained SiGe on Si. The challenge is the material quality of the strained SiGe and strained Si layers. Defect free layer growth is only possible up to a critical thickness. Above this critical thickness the layers start to relax which goes together with the unwanted formation of defects (misfit dislocations and threading dislocations) in the active layer. In addition, post-epi fin patterning is known to result in an elastic layer relaxation.
The epitaxial growth of strained SiGe on Si substrates is well understood. Layer relaxation during epitaxial growth strongly depends on epitaxial growth conditions. E.g. the critical thickness varies as function of growth temperature (the critical thickness increases with decreasing growth temperature). Another important parameter is the conditioning of the starting surface on top of which the strained layers are grown. Contamination on the starting surface reduces the critical thickness. The move from Si substrates to SiGe SRBs complicates the issue. The starting surface of the SiGe SRB has some imperfections and there is also a need to reduce process temperatures. This makes it e.g. more challenging to remove the native oxide from SiGe SRB starting surfaces on top of which the strained Si and SiGe layers need to be grown.
Within the frame if this project, the candidate will study the material properties of compressive strained Si1-xGex (x ~50%) on Si0.75Ge0.25-SRBs and compare the layer relaxation with its Si0.75Ge0.25/Si-substrate counterpart. A Design of Experiments will be used to extract the critical thickness as function of the growth conditions and the surface preparation of the SiGe-SRB starting surface. In addition, possible layer relaxation during post-epi thermal processing will be studied.

Type of project: Internship or thesis project

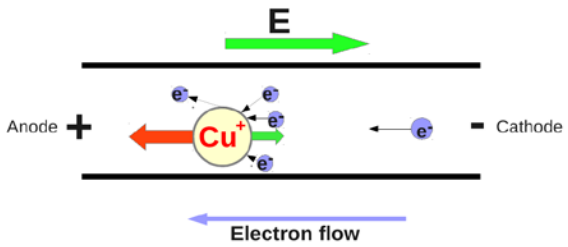
Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Materials Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Robert Langer (Robert.Langer@imec.be), Clement Porret (Clement.porret@imec.be) and Roger Loo (roger.loo@imec.be).

Study of electromigration mechanisms in advanced nanoelectronics interconnects by means of low-frequency noise measurements

Electromigration (EM) is the mass transport of metal ions caused by a momentum exchange between accelerated electrons and the diffusing metal atoms in a conductor. In other words, electrons that are accelerated by the electric

field that is applied to the conductor, collide with its metal ions and thereby push them from the cathode to the anode side. This results in void formation at the cathode and accumulation of material (so called hillocks) at the anode.



Since EM causes sudden failure of the interconnect lines, it can drastically decrease the reliability of an entire electronic component. Because of the continuous downscaling of interconnect dimensions, electromigration becomes increasingly problematic. To prevent EM, it is key to identify the fast diffusion mechanisms by which the metal ions can be transported and a good Em characterization technique is required. The present, generally accepted EM test method already dates from the 1960's and makes use of the fact that EM is accelerated at elevated temperatures and by high current densities [1]. Notwithstanding this method reduced test times form several years to months or even weeks, there are still many drawbacks; many test samples are required, it is destructive, still quite time consuming and limited in providing adequate physical understanding [2]. Therefore, we are working on a new EM test method which is based on low-frequency (LF) noise measurements. These LF noise measurements allow a direct calculation of the activation energy of diffusion paths that are important for EM failure. Moreover, it is possible to discern several EM mechanisms from each other, whereas in classic tests the measured activation energy can be an average of several mechanisms rather than one specific [3]. Finally we have demonstrated that the EM lifetimes can be predicted by LF noise measurements [4].
Your work will consist of performing low-frequency noise measurements and standard accelerated tests on various advanced micro-electronics interconnects in order to gain understanding regarding their electromigration mechanisms. Moreover, you will be directly involved in the improvement and further development of this new test method to make it suitable for industrial application.

[1] J. R. Black, "Electromigration: A brief survey and some recent results," Electron Devices, IEEE Transactions on, vol. 16, no. 4, pp. 338–347, 1969.
[2] J. Lloyd, "Black's law revisited: Nucleation and growth in electromigration failure," Microelectronics Reliability, vol. 47, no. 9-11, pp. 1468–1472, 2007.
[3] S. Beyne, K. Croes, I. De Wolf, and Z. Tokei, "1/F Noise Measurements for Faster Evaluation of Electromigration in Advanced Microelectronics Interconnections," Journal of Applied Physics, vol. 119, no. 18, p. 184302, 2016.
[4] S. Beyne, K. Croes, I. D. Wolf, and Z. Tokei, "Direct Correlation between Low-Frequency Noise Measurements and Electromigration Lifetimes," The international Reliability Physics Symposium, 6B-3, 2017.

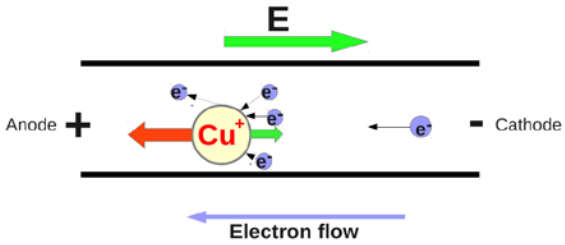
Type of project: Internship or thesis project or combination of both with a minimum duration of 3 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Materials Engineering, Nanoscience & Nanotechnology, Physics, Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Sofie Beyne (sofie.beyne@imec.be).

Development of a new electromigration test method for advanced nanoelectronics interconnects

Electromigration (EM) is the mass transport of metal ions caused by a momentum exchange between accelerated electrons and the diffusing metal atoms in a conductor. In other words, electrons that are accelerated by the electric field that is applied to the conductor, collide with its metal ions and thereby push them from the cathode to the anode side. This results in void formation at the cathode and accumulation of material (so called hillocks) at the anode.



Since EM causes sudden failure of the interconnect lines, it can drastically decrease the reliability of an entire electronic component. Because of the continuous downscaling of interconnect dimensions, electromigration becomes increasingly problematic. To prevent EM, it is key to identify the fast diffusion mechanisms by which the metal ions can be transported and a good Em characterization technique is required. The present, generally accepted EM test method already dates from the 1960's and makes use of the fact that EM is accelerated at elevated temperatures and by high current densities [1]. Notwithstanding this method reduced test times form several years to months or even weeks, there are still many drawbacks; many test samples are required, it is destructive, still quite time consuming and limited in providing adequate physical understanding [2]. Therefore, we are working on a new EM test method which is based on low-frequency (LF) noise measurements. These LF noise measurements allow a direct calculation of the activation energy of diffusion paths that are important for EM failure. Moreover, it is possible to discern several EM mechanisms from each other, whereas in classic tests the measured activation energy can be an average of several mechanisms rather than one specific [3]. Finally we have demonstrated that the EM lifetimes can be predicted by LF noise measurements [4].
Before this test method can be applied in the semiconductor industry, it is important to understand whether the LF noise measurements are indeed non-destructive. During this internship you will perform LF noise measurements on sub-micron interconnects and investigate whether they affect the electromigration properties of the samples by doing also standard accelerated EM tests. Based on your findings, the test conditions can then be modified in order to make the LF noise measurements suitable for industrial use.

[1] J. R. Black, "Electromigration: A brief survey and some recent results," Electron Devices, IEEE Transactions on, vol. 16, no. 4, pp. 338–347, 1969.
[2] J. Lloyd, "Black's law revisited: Nucleation and growth in electromigration failure," Microelectronics Reliability, vol. 47, no. 9-11, pp. 1468–1472, 2007.
[3] S. Beyne, K. Croes, I. De Wolf, and Z. Tokei, "1/F Noise Measurements for Faster Evaluation of Electromigration in Advanced Microelectronics Interconnections," Journal of Applied Physics, vol. 119, no. 18, p. 184302, 2016.
[4] S. Beyne, K. Croes, I. D. Wolf, and Z. Tokei, "Direct Correlation between Low-Frequency Noise Measurements and Electromigration Lifetimes," The international Reliability Physics Symposium, 6B-3, 2017.

Type of project: Internship project with a minimum duration of 2 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Materials Engineering, Nanoscience & Nanotechnology, Physics, Electrotechnics/Electrical Engineering

Responsible scientist(s):

For further information or for application, please contact Sofie Beyne (sofie.beyne@imec.be).

II. Image Sensors and Vision Systems

High speed column ADC for CMOS Image sensors

CMOS image sensors have made capturing images ubiquitous in our everyday life. Lower cost and power have supported common deployment in mobile devices, but also in many other applications CMOS image sensors have replaced the analog CCD solutions. Sensors now allow analysis of many thousands of images per second, and new applications are enabled by more integrated functionality and more data provided by these sensors. Imec develops specialty image sensors to enable new frontiers in imaging. While there is a continuous push for higher speed, enabled by our high speed imaging platform, scientific applications also demand higher resolution and lower readout noise. This pushes the boundaries for all parts of the readout circuitry. Here, the column ADC is a key analog building block. The limited available chip area (thousands of parallel ADCs are needed) and high immunity to coupling on chip (thousands of circuits coupling together) make this ADC design very different from a conventional design and thus very challenging. On the other hand, these ADCs can benefit from shared resources to increase efficiency. In this thesis, we will look at current state-of-the art column ADCs and come up with a new architecture that pushes the speed to the next generation applications, while maintaining the same resolution. This thesis will start with a literature survey and targets finalizing an ADC circuit design for these applications.

Type of project: Internship or thesis project or combination of both with a minimum duration of 7 months

Degree: Master majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Maarten De Bock (Maarten.DeBock@imec.be), David San Segundo Bello (David.SanSegundoBello@imec.be) and Annachiara Spagnolo (Annachiara.Spagnolo@imec.be).

Highly efficient row drivers for TDI Image sensors

CMOS image sensors have made capturing images ubiquitous in our everyday life. Lower cost and power have supported common deployment in mobile devices, but also in many other applications CMOS image sensors have replaced the analog CCD solutions. However, for some applications, CCD still has some very interesting advantages. One such application is time-delay-integration (TDI). Here, the active photodiode is electronically moved along with the moving subject. This results in a longer time window for which a high speed moving object is "still" with respect to that photodiode. As a result, more light can be collected from that subject and the SNR of the image increases which makes this type of sensor very attractive in low light conditions. Imec has developed CDD-in-CMOS, to further enhance this CCD operation with CMOS readout electronics. This pushes the speed boundaries for these TDI applications even further, and larger pixel arrays with higher readout speeds are now demanded by our customers. As a consequence, a lot of power is also burned when driving the large capacitive load presented by the CCD gates. In these thesis, we want to investigate how we can drive the CCD gates more efficiently and in a scalable manner for larger pixel arrays, e.g. by exploiting the unique multi-phase control signals that are required for CCD operation. This thesis will start with a literature survey and targets finalizing a driver circuit design for these applications.

Type of project: Internship or thesis project or combination of both with a minimum duration of 7 months

Degree: Master majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Maarten De Bock (Maarten.DeBock@imec.be), David San Segundo Bello (David.SanSegundoBello@imec.be) and Philippe Coppejans (Philippe.Coppejans@imec.be).

Readout electronics for ultra high-speed imaging

Consider the research that led towards the detection of the Higgs Boson, also known as the "god particle". This research performed at CERN has contributed to our understanding of the world as it is and as it came to be. In order to confirm the theory about this particle that gives mass to matter, scientists have accelerated charged carriers to velocities close to the speed of light. At these speeds they have ultra-high energy so that collisions allow us insights in otherwise hidden physics. One of the key technologies allowing for the detection of such particles is ultra-fast imaging (GHz). Next to fundamental research in collider experiments, ultra-high speed imaging finds application in numerous fields such as life-science imaging (spectroscopy, lab-on chip, tomography), material sciences (crack propagation), combustion research or fusion reaction diagnostics. IMEC develops these speciality image sensors to enable new frontiers in imaging.
In the context of CMOS image sensors, this thesis will focus on the design of a CMOS readout circuitry for ultra high-speed applications. The thesis will start with a literature survey and targets finalizing a silicon design.

Type of project: Thesis project with a duration equivalent to 6 full months

Degree: Master in Engineering majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Andreas Süss (andreas.suess@imec.be) and Linkun Wu (linkun.wu@imec.be).

Readout electronics for single photon imaging

Imagine seeing individual photons. This access to quantum information would enable you to study phenomena such as quantum entanglement which can be employed in quantum cryptography. You could investigate correlations of photon-trails which would enable you to better surpress ambient noise and highlight the actual information. Seeing individual photons is a technology believed to revolutionize life-science imaging applications (spectroscopy) and to enable range detection for autonomous driving. Also it would allow you to see things at unprecidented sensitivity which would enable you to see ultra-low light levels as they occur e.g. in life-science (multi-photon imaging), night vision and alike. As of a few years, CMOS compatible photodetectors are able to detect single impinging photons and convert them into a voltage signal. As these arrive with high rates, dedicated readout circuitry is required to process the information. IMEC develops these speciality image sensors to enable new frontiers in imaging.
In the context of CMOS image sensors, this thesis will focus on the design of a CMOS time-to-digital converter for readout of single-photon detectors. The thesis will start with a literature survey and targets finalizing a silicon design.

Type of project: Thesis project with a duration equivalent to 6 full months

Degree: Master in Engineering majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Andreas Süss (andreas.suess@imec.be) and Philippe Coppejans (Philippe.Coppejans@imec.be).

Thin film-based image sensors

Image sensors and vision system development is always demanding for higher resolution, sensitivity, dynamic range, along with smaller chip size. These demands push the pixel pitch below 1 µm and drive advanced CMOS imaging technology development to improve low light sensitivity and saturation level. Scaling the pixel pitch below 1µm reduces the photo-sensitivity, device full-well capacity and fill-factor to unacceptable levels. Moreover, a key

requirement for the employment of imagers in machine vision systems is the ability to see beyond the visible spectrum and through obstacles, enabling night vision and hidden targets recognition. The solution to the CMOS limitations is presented by the vertical stack of a photo-sensitive material such as a thin-film material or a compound semiconductor on the CMOS substrate. These layers show much higher saturation levels, infra-red IR sensitivity and allow to keep the photodetector separated from the silicon substrate. However, the thin film devices exhibit much higher dark current values and require a different biasing approach with respect to the CMOS photodiodes. Furthermore, the single sampling readout conventionally used shows a very high read noise, while the use of multiple sampling techniques increases the system memory requirements and reduces the readout speed. The focus of this internship will be on the design of building blocks of the readout chain for a thin-film-photo-detector (TFPD) image sensor. An initial phase of architectural study will be followed by an exploration of innovative ways to readout TFPDs. The final goal is a new complete circuit design for a TFPD readout.

Type of project: Internship with thesis project with a minimum duration of 6 months

Degree: Master majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Fortunato Frazzica (Fortunato.Frazzica@imec.be) and Maarten De Bock (Maarten.DeBock@imec.be).

III. Silicon Photonics

Process development and characterization of devices based on ferroelectric oxides for silicon photonics applications

Transistor scaling is increasing the chip density making inter- or intra-chip data transmission by electrical wires more challenging. Silicon photonics interconnects are promising to deliver the increasing bandwidths required at shorter distances, lowering the power consumption. Therefore, silicon photonics devices such as photodetectors, modulators and switches have been recently developed. Ferroelectric oxides with large Pockels coefficient have attracted interest for power-efficient electro-optical devices. Achieving high performance silicon photonics devices based on such materials is still challenging and requires excellent material control during the epitaxial growth and also during device fabrication. In this project the student will be involved in the design and fabrication of basic structures on ferroelectric oxides in imec's experimental clean-room and also in the electrical and optical characterization of these devices. The student will learn to perform processing steps such as optical lithography, wet and/or dry etching, annealing, and the deposition of metal contacts for the fabrication of devices. After fabrication the student will learn to characterize the devices and extract material parameters via electrical, optical and electro-optical measurements. The candidate will obtain multidisciplinary knowledge on material science, semiconductor processing techniques and analysis. This project is open to self-supported students only (no imec allowance will be provided).

Type of project: Internship or thesis project or combination of both
This project is open to self-supported students only (no imec allowance will be provided).

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Electrotechnics/Electrical Engineering, Physics, Materials Engineering, Nanoscience & Nanotechnology, Chemistry/Chemical Engineering

Responsible scientist(s):
For further information or for application, please contact Marianna Pantouvaki (Marianna.Pantouvaki@imec.be) and Mark Hsu (Min.Hsiang.Hsu@imec.be).

Reliability behavior of Germanium waveguide photodetectors

Photodetectors (PDs) integrated in a silicon photonics platform offer great potential to improve the power budget of Si-based optical interconnects, where low-voltage germanium waveguide PDs with a gain × bandwidth product over 100GHz are demonstrated (Figure 1 and [1,2]).

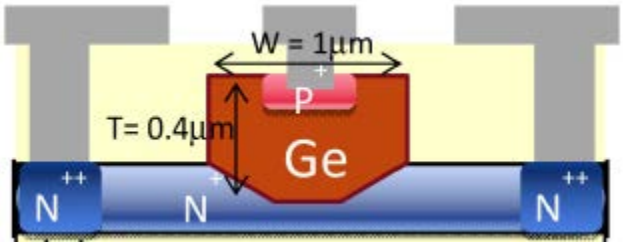


Figure 1

During operation at use conditions, such photodetectors are being supplied with a low bias-voltage in reverse mode, where its dark current needs to remain at a low level.
The development of accelerated tests methods and the understanding of the reliability degradation mechanisms of a specific design of such a PD are the topic of this project.
The student will need to a) built physical models to explain degradation of the PD under study based on own and existing results b) perform needed electrical tests to investigate and c) analyze and present the obtained data.
The student will be able to collaborate with device, integration and reliability experts in imec.

[1] H. T. Chen, J. Verbist, P. Verheyen, P. De Heyn, G. Lepage, J. De Coster, Ph. Absil, B. Moeneclaey, X. Yin, J. Bauwelinck, J. Van Campenhout and G. Roelkens, "Sub-5V Germanium Waveguide Avalanche Photodiode based 25 Gb/s 1310 nm Optical Receiver", Asia Communications and Photonics Conference, pp. AM1B.4, 2015
[2] H. T. Chen, J. Verbist, P. Verheyen, P. De Heyn, G. Lepage, J. De Coster, P. Absil, X. Yin, J. Bauwelinck, J. Van Campenhout and G. Roelkens, "High sensitivity 10Gb/s Si photonic receiver based on a low-voltage waveguide-coupled Ge avalanche photodetector", Optics Express, Vol. 23, No. 2, pp. 815, 2015

Type of project: Internship project with a duration of 6 to 9 months

Degree: Master in Science majoring in Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Kristof Croes (Kristof.Croes@imec.be) and Alicja Lesniewska (Alicja.Lesniewska@imec.be).

Development of a parallel test method for wafer-level characterisation of silicon photonics devices

Photonics, the science of generating and/or processing light waves on a micrometer-scale, is enabling evermore applications, including LED-lighting, fiber-to-the-home internet, solar panels, displays and image sensors. Recent progress in nano-fabrication now also allows to produce large-scale photonic circuits on wafer-scale using the infrastructure of the electronics industry, providing cost-effective high-quality optical systems. Imec is playing a crucial role in the development of wafer-scale photonics, and already developed a state-of-the-art silicon photonics (SiP) platform for high-speed optical communication and sensing.
To complement this silicon photonics technology platform, an optical measurement lab has been set up with dedicated measurement tools that enable comprehensive electrical and optical wafer-scale characterisation of the SiP technology components.
So far the optical wafer-level characterisation has always been carried out using a pair of single mode (SM) fibers to couple light into the optical input port of a circuit and to collect light at the optical output port. The next step in the development of our optical measurement capabilities will be the parallellization of optical measurements using an array of optical fibers, allowing to measure multiple optical circuits simultaneously. This new test approach brings about a number of challenges in several domains:

- Mechanical: alignment of the fiber array to the fiber grating couplers using a 6-degree-of-freedom motorized fiber manipulator
- Optical and electrical: configure measurement instruments for synchronized data acquisition, and optimize measurement throughput.
- Design: optical and electrical configuration of the test equipment is closely linked to the actual design of the optical component test sites and the type of devices measured. Interaction with the design team is therefore essential in order to come to an optimized test setup and test site layout.
- System calibration and data analysis: methods for calibrating the optical properties of the test setup, acquiring and analyzing data across multiple channels will have to be established.

All of the above will obviously require significant effort for expanding the capabilities of our existing optical measurement software environment, which is using the engineering-standard Python scripting language. We are looking for two students who will work on the above based on their interest and experience. This is a hot topic in

the growing integrated photonics industry, hence the students will collaborate closely with imec's design and test engineers.

Type of project: Internship project

Degree: Master majoring in Nanoscience & Nanotechnology, Physics, Mechanical Engineering, Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Jeroen De Coster (Jeroen.DeCoster@imec.be) and Peter De Heyn (Peter.DeHeyn@imec.be).

IV. Thin-Film Flexible Electronics

Optical design of infrared thin-film photodetectors

Most modern infrared photodiode arrays combine a silicon based backplane with an infrared absorbing material. These thick substrates are flip-bonded to the backplanes, which limits the pixel resolution. Processing directly on top of a silicone backplane will increase the pixel density and decreases the production cost. At the same time, this solution will create options to fabricate flexible photodetectors, processing the infrared materials on sheets in combination with flexible electronics. In the recent years, colloidal quantum dots received an increasing amount of attention due to their opto-electronic properties, with applications in light-emitting diodes and photovoltaics. Once the size of a nanoparticle reaches the exciton Bohr radius, quantum confinement effects will affect both the light absorption and emission spectrum of the material. By starting from a bulk material with infrared absorbing properties, one can obtain visible or infrared absorbing quantum dots. The quantum dots are typically surrounded by organic ligands that stabilize the material. The material can be made soluble by selecting the correct ligand. Moreover, these ligands can limit the large surface recombination inherent to the small quantum dots. The focus of this internship will be on the optical aspects of such an IR absorbing stack. The involved layers will be measured using ellipsometry to obtain the complex index of refraction, depending on the ligand termination. Using a custom build transfer matrix based optical simulator, you will determine the best stack layout for the highest performance. These stacks will be matched with experimental values. If applicable, the student will receive training on the relevant processing and characterization tools. After a short introduction to the facilities, an independent investigation is expected with the focus on short-term research goals.

Type of project: Thesis with internship project with a minimum duration of 6 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Electrotechnics/Electrical Engineering, Materials Engineering, Nanoscience & Nanotechnology, Computer Science

Responsible scientist(s):
For further information or for application, please contact David Cheyns (David.cheyns@imec.be) and Pawel Malinowski (Pawel.malinowski@imec.be).

Organic patterning

The ever-increasing resolution of displays and imagers fabricated using organic semiconductors requires new, advanced patterning techniques. Currently, the most popular fabrication process for high-resolution displays based on thermally-evaporated OLED stacks is shadow-masking. Still, this technology has limitations in terms of the smallest feature size and up-scalability for very large substrate sizes. As an alternative, dedicated photolithography processes can be used. In this case, special care needs to be taken to ensure chemical compatibility of the processing products used with the very fragile organic compounds. Imec is active in developing novel solutions enabling patterning of advanced organic semiconductor devices by photolithography. The focus of this internship will be optimization of the fabrication process of high-resolution organic photodetectors and light emitting diodes. Active layers will be deposited by spin-coating (solution processed polymers) or thermal evaporation (evaporated small molecules). The student will be involved in the entire fabrication cycle, performed in the state-of-the-art facilities including imec's cleanroom and dedicated organic line. Initially, the student will receive training on the relevant processing and characterization tools. After a short introduction to the facilities, an independent investigation is expected with the focus on short-term research goals. As this internship is focused on the photolithography aspects of the semiconductor fabrication route, experience in this domain is a necessity.

Type of project: Internship project with a minimum duration of 6 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Electrotechnics/Electrical Engineering, Materials Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Pawel Malinowski (Pawel.malinowski@imec.be) and TungHuei Ke (Tung.Huei.Ke@imec.be).

Investigation of different source-drain metal integration in a-IGZO TFT structures

Amorphous oxide semiconductors (AOSs) are of great interest for thin-film transistor (TFT) channel layer applications. They have been studied due to their superior characteristics, such as high uniformity, high electron mobility (10-50 cm2/V·s), and their fabrication at low temperatures on plastic substrates. These advantages of a-IGZO TFTs are promising for next-generation backplanes for displays and circuits on the transparent and flexible substrate. Currently in our self-aligned (SA) TFTs, the S/D metal is integrated with few limitations on the minimum metal line dimensions (feature size and thickness) and resistivity. For the future large area applications, the S/D metal line dimensions and resistance (contact and line) need to be reduced. The objective of this internship is to integrate different low resistive S/D metals using etch process in the SA and dual-gate TFTs. The student investigates both wet and dry (fluorine and chlorine based chemistry) etch methods. The integration also includes the change in the intermetal layer if required. Excellent TFT characteristics of the final TFT stack on the flexible substrate are expected. From the results a conclusion need to be drawn on the integration issues and material of the S/D metal layer. This activity also includes the measurements of the fabricated devices.

Type of project: Internship project

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Materials Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Manoj Nag (Manoj.nag@imec.be) and Kris Myny (Kris.Myny@imec.be).

Organic light emitting diode (OLED) with high stability

Organic light emitting diode (OLED) is the most well-known organic electronics in the display and lighting industry. It is light-weight, low power, with wide viewing angle and fast response time, which is very promising for the display of portable electronics. Furthermore, it can be integrated with flexible back-plane panel for flexible active matrix OLEDs (AMOLEDs) display. For OLED device, it is very sensitive to ambient environment, especially water and oxygen. It is necessary to develop stable OLED stacks for varies process conditions. The goal of this internship is to develop a stable OLEDs stack with good device performance for different applications. Task description:1. Development of highly thermal stable OLED stack for long hour heating treatment: Organic semiconductors with high thermal stability will be evaluated in OLED devices. The developed OLED stacks will be applied in a back-plane panel with thin-film encapsulation for demonstration of flexible AMOLEDdisplay.2. Study the impacts of all kinds of process on the OLEDs stacks. Different kind of measurements including photophysical properties like PL and PLQY or excited state lifetime and device reliability tests would be investigated.

Type of project: Internship project with a minimum duration of 6 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Materials Engineering, Physics, Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact TungHuei Ke (Tung.Huei.Ke@imec.be).

Integrated organic thin film transistors for circuits application

Flexible electronics have drawn many attentions for its applications in large area electronics, such as flexible display. To realize the complex circuits on foil, high performance thin film transistors (TFTs) with low process temperature are required. Metal oxide n-type transistors have been demonstrated in industry with average mobility around 15 cm2/V·s for back-plane applications in flexible display and OLED TV. However, there is no p-type TFTs demonstrated with the process temperature lower than 150 °C in metal oxide TFTs. Instead, organic TFTs have also been widely studied for its advantages, such as low process temperature and nice p-type TFTs performance. Record high p-type mobility up to 30 cm2/ V·s has been demonstrated in large area electronic by solution proceed single crystal organic TFTs. Thus OTFTs has its potentials in high performance p-type logic circuits and also CMOS application in cooperation with n-type metal oxide transistors. To realize high performance TFTs in large area electronics, contact resistance of the TFTs is a very important factor that limits the performance of the OTFT circuits. With the improvement in contact resistance in OTFTs, many performance issues would be improved e.g. speed of circuits, noise margin in CMOS logic gates and self-heating induced instability. In the project, you will be part of the transistor team and you will process and characterize the organic thin-film transistors independently with some initial training. You will start with device fabrication by working with vacuum deposition system and photolithography for different process steps. Different device structures would be investigated. You will electrically characterize the TFTs and interpret the data to define follow-up experiments. The morphologies of the devices maybe characterized by different technologies such as optical microscopy, atomic force microscopy (AFM) and x-ray diffraction (XRD). This project is very practical and process oriented. Fundamental knowledge of TFT device physics is necessary. A good sense of experimental design and discipline to execute the plan are required. Persons with hands-on experience in labs or cleanrooms are preferred. Independent working style and good communication abilities in English are highly appreciated.

Type of project: Internship project with a minimum duration of 6 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Materials Engineering, Physics, Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact TungHuei Ke (Tung.Huei.Ke@imec.be).

Vacuum deposited perovskite for p-type TFT

Amorphous oxide thin film transistors (TFTs) such as InGaZnO are widely used in high performance display backplanes. It is due to the fact that n type InGaZnO TFTs have high mobility, high on/off ratio and low fabrication temperature. However, due to the lack of a good p-type oxide TFT, a low-power high-speed CMOS circuits based on oxide semiconductor cannot be realized. Therefore, successful development of high performance p type oxide TFTs can enable many new application fields.
In p-type thin film metaloxide semiconductor , the valence band maximum of oxide semiconductor is mainly composed by 2p orbitals of oxygen atoms. Those localized 2p orbital states limit the hole mobility. For that reason, s or d orbitals of metals are used to delocalize the 2p orbital state resulting in high hole mobility oxide semiconductor. To date, several p-type oxide materials have been reported for instance Ni, Cu based materials for d block and Sn, Bi based materials for s block. Unfortunately p-type thin film oxide semiconductors have usually a low oxidation state. As consequence, these materials are difficult to integrate in manufacturing processes, resulting in unstable TFT properties and high-off current.
The target of this internship is to develop vacuum deposited perovskite p-type semiconductor which are stable and have high hole mobility. Binary and ternary semiconductor materials will be co-deposited by thermal evaporation processes. TFTs will be fabricated and electrically characterized. This internship topic requires a precise and hard-

working student who will have the chance to work in a professional research environment and get experience in process development in a state-of-art cleanroom environment.

Type of project: Internship or thesis project or combination of both with a minimum duration of 6 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Materials Engineering, Physics, Electrotechnics/Electrical Engineering, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Soeren Steudel (soeren.steudel@imec.be) and Mai Phi Hung (Phi.Hung.Mai@imec.be).

V. Life Sciences

Software development and signal processing for high throughput silicon multi-electrode array systems

Cardiotoxicity is the major cause of drug withdrawal from the market, despite rigorous toxicity testing during the drug development process. This puts an enormous risk and pressure on pharmaceutical companies. Existing safety screening techniques (optical, impedance, cellular assays) are either too limited in throughput or offer too poor predictability of toxicity to be applied on large numbers of compounds in the early stage of drug development. At imec, a new silicon multi-electrode array chip platform is developed that will address those challenges. This chip needs to be steered through a system that allows for amongst other features: electrode selection, uploading stimulation and recording parameters, controlling fluidic flow, customized user settings, etc. The intern project consists of the development of the graphical user interface for addressing chip functionality, high data rate transfer, (biological) data visualization, driver and USB communication, trouble shooting, multi-threading programming, etc. Advanced automated signal processing for in vitro cardiac signals and sorting will also be needed. We are looking for strong candidates with excellent knowledge of Visual studio C#, .Net, Matlab or Python. Understanding of VHDL and FPGA programming is a plus, as well as experience with biological signal processing.

Type of project: Internship or thesis project or combination of both with a minimum duration of 6 months

Degree: Master in Science or Master in Engineering majoring in Computer Science, Electrotechnics/Electrical Engineering, Physics

Responsible scientist(s):
For further information or for application, please contact Veerle Reumers (Veerle.reumers@imec.be) and Dries Braeken (dries.braeken@imec.be).

Single cancer cell characterization using high-density microelectrode arrays

Cancer research literature has increased dramatically over recent decades due to increasing knowledge in molecular biology and genetics of the disease. However, current experimental methods are mostly performed on relatively large populations of cells obscuring the large heterogeneity in cancer cells, even within single solid tumor samples. The ability to analyze cells with single-cell precision is crucial for the investigation of rare cell subpopulations within tumors and could over time result in the development of improved cancer therapeutics. In recent years, imec developed an advanced CMOS microelectrode array chip to analyze single cancer cells using electrical impedance spectroscopy. This technique is based on fundamental electrical properties of biological cells and can be used for cell characterization, cell status monitor and drug screening in heterogeneous cell populations. The purpose of this research project is to investigate differences in the impedance spectra of cancer cell lines and statistically process these results in order to gain knowledge about the biology of different cancer cell lines. The research project consists partly of experimental work done in the lab and party of data processing. Data analysis is of major importance in this research project, since differences in these impedance spectra are typically small. Artificial neural networks have been used recently to distinguish different cell lines, but other machine learning techniques can be applied if these yield a better results. Data (pre-)processing and statistical analysis have traditionally been performed using MATLAB, but Python or R could also be used if preferred by the student.

Type of project: Internship or thesis project or combination of both with a minimum duration of 6 months

Degree: Master in Science or Master in Engineering majoring in Bioscience Engineering, Electrotechnics/Electrical Engineering, Physics, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Carl Van Den Bulcke (Carl.vandenbulcke@imec.be) and Dries Braeken (dries.braeken@imec.be).

Electrical impedance assay for bacterial biofilm detection

Bacterial biofilms are complex surface-associated communities of microorganisms embedded in a self-produced matrix. Within a biofilm, bacteria are up to 1000 times more tolerant to antibiotics and disinfectants. As a consequence, biofilms cause very persistent contaminations and infections. Nowadays there is a high need for in-situ detection techniques, e.g. on implants, on catheters, or in industrial piping systems, that would reduce the costs that biofilm formation causes. At imec, we are developing microelectrode-based impedance sensors that allow for in-situ biofilm monitoring. Currently, we have optimized an impedance sensing assay to detect and characterize bacterial biofilm formation using microelectrode arrays. The student involved in this project will be responsible for performing experiments as well as processing the data. The experimental work involves confocal microscopy, electrochemical measurements and bacteria culture techniques. Besides, the output data will be analysed by combining electrical circuit modelling and data mining.

Type of project: Internship or thesis project or combination of both with a minimum duration of 6 months

Degree: Master in Science or Master in Engineering majoring in Computer Science, Electrotechnics/Electrical Engineering, Physics

Responsible scientist(s):
For further information or for application, please contact Erkuden Goikoetxea (Erkuden.goikoetxea@imec.be) and Dries Braeken (dries.braeken@imec.be).

Mesoporous materials for biosensing applications

Biosensor devices are revolutionizing modern health-care as they enable to detect disease markers (e.g. protein biomarkers) in clinical samples. An electrochemical biosensor is an analytical device containing immobilized bioreceptors (e.g. an enzyme, antibody, DNA or even whole cells or tissues) in close contact with an electrochemical transducer that converts a biological recognition event into a quantitatively measurable electrical signal. Two key requirements that still are to be improved in the development of electrochemical biosensors are (i) the need for a robust and reliable immobilization of large amounts of biomolecules, and (ii) a favorable environment for efficient electron transfer reactions. Mesoporous materials display several attractive properties to circumvent both problems: they have a large surface area for the immobilization of bio-molecules and/or reactants, a widely open and interconnected porous structure and they often display intrinsic catalytic and/or conductive properties.
These qualities of mesoporous silica will be exploited to fabricate a sensitive electrochemical biosensor. Ordered mesoporous materials will be prepared by using a so-called 'template' route involving the hydrolysis and condensation of silicon alkoxide precursors in the presence of a supramolecular template, usually a surfactant. Various ionic or non-ionic surfactants or water-soluble polymers will be used to prepare well-ordered mesoporous silica, with monodisperse pore sizes ranging between 2 – 10nm. In addition, pore-expanders can be used to reach bigger pore sizes. Moreover, the surface of the pores can be further functionalized using self-assembled monolayers of organosilanes. The resulting mesoporous layers will be characterized using different analytical techniques (e.g. XRD, FTIR, XPS, ellipsometry, AFM, ...). In a second phase, the efficacy of mesoporous layers as suitable immobilization matrices for proteins while preserving their biological activity, will be evaluated. Finally, as a proof-of-concept, these mesoporous layers will be incorporated on a metal electrode in order to construct a simple electrochemical biosensor.

Type of project: Thesis project or combination of thesis with internship with a minimum duration of 3 months

Degree: Master in Engineering Technology, Master in Science or Master in Engineering majoring in Bioscience Engineering, Chemistry/Chemical Engineering, Materials Engineering, Nanoscience & Nanotechnology
Responsible scientist(s):
For further information or for application, please contact Rita Vos (vos@imec.be), Tim Stakenborg (stakenborg@imec.be) and Karolien Jans (jansk@imec.be).

Photonic modulators

Photonics, the science of generating and/or processing light waves on a micrometer-scale, is enabling evermore applications, including LED-lightning, fiber-to-the-home internet, solar panels, displays and image sensors. Recent progress in nano-fabrication now also allow to produce large-scale photonic circuits on wafer-scale with CMOS-compatible processes, providing cost-effective high-quality optical systems. Imec is playing a crucial role in the development of wafer-scale photonics, and already developed a state-of-the-art silicon photonics platform for high-speed optical communication and sensing (Fig.1). Recently, we started developing an additional platform for visible photonics targeting applications in industrial and biomedical sensing. While this platform already supports stable static photonic components, dynamic components still need to be developed. Phase modulators are crucial for dynamic photonics. They control and change the phase of guided light waves, and hence enable on-chip (spatial) switching of light, as well as beam shaping and steering.

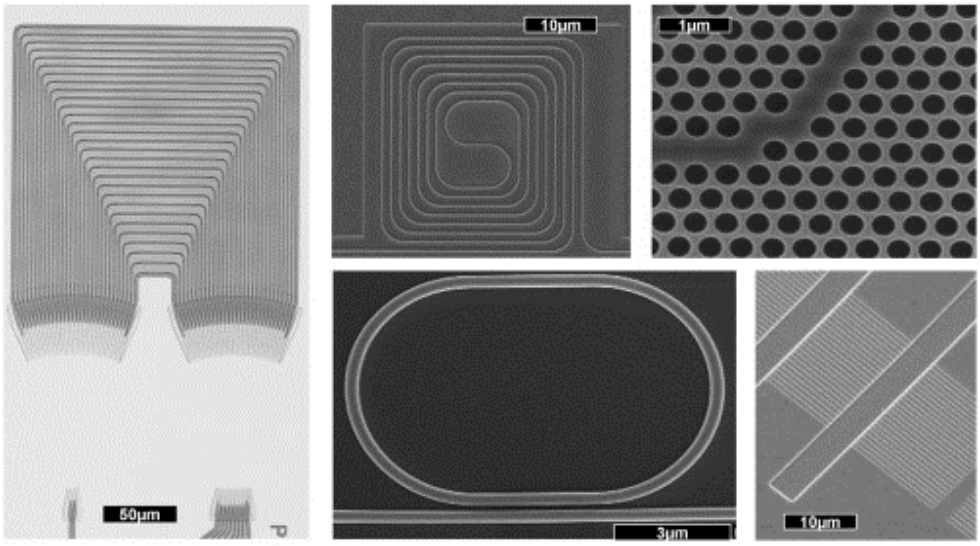


Fig.1 scanning electron micrograph of optical filters fabricated on wafer-scale at imec

The goal of this project is to develop a photonic phase modulator for imec's newest technology platform. This includes the following project phases:

1. Compare different modulator principles and chose the most applicable one, taking into account technological constraints and applicability.
2. Design a modulator using powerful computer-aided-design tools
3. If your design proves to be promising, you can fabricate it in our clean rooms
4. Characterize your prototype, closing the loop with your original design

This project allows you to learn different aspects of (photonic) chip development in an application-oriented environment.

Type of project: Internship or thesis project or combination of both with a minimum duration of 8 weeks

Degree: Master in Science or Master in Engineering majoring in Electrotechnics/Electrical Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Bruno Figeys (Bruno.figeys@imec.be) and Tom Claes (tom.claes@imec.be).

Single molecule sensing by nanopore field-effect transistors

Nanopore-based DNA sequencing technology has made the step from fundamental research to application. In the last few years, it has been used for the in-field analysis of Ebola in Africa as well as bio-objects in the NASA Space Place.
Still today, a remaining intrinsic challenge for nanopore sensing is its weak and indistinctive output signals and the lack of scalability and parallelization. In this project, we will take an exciting adventure on single molecule sensing by nanopores and will study a feasible way for solving the challenge. We propose a novel sensing system based on nanopore field-effect transistor sensors, in which a single molecule can be confined and aligned by nanopore fluidics to the most sensitive region of an advanced silicon transistor. Such a nanopore FET combines field effect modulated potentiometric amplification with a very precise location, and is intrinsically more sensitive and intense than the amperometric sensing in nanopores. We expect this technology will have direct impact on point of care biomedical research, diagnostics and precision medicine.
We expect a candidate student who has interests on and is self-motivated for combining transistor technologies with nanopore sensing. The work contains both single molecule experiments and simulations combining nanofluidics with advanced transistor modelling.

Type of project: Thesis project

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Electrotechnics/Electrical Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Chang Chen (chang.chen@imec.be) and Pol Van Dorpe (pol.vandorpe@imec.be).

Characterizing bio-molecular interactions using fluorescence depolarization

Silicon photonics has become one of the most promising photonic integration platform in the recent years. The combination of high-index-contrast and compatibility with CMOS processing technology made it possible to use the electronics fabrication facilities to make photonic circuitry. There has been a tremendous interest towards integration of photonic devices in biological sensing and detection recently. The visible and near-infrared (500-950 nm) wavelength window is of great interest for this kind of applications due to low photo damage and availability of low cost sources-detectors. Unlike Silicon, Silicon Nitride (SiN) is transparent in this Visible & Near-Infrared window and provides the combination of high-index-contrast and compatibility with CMOS processing technology. A low-loss SiN platform has been developed in the last years at imec.
In this thesis, the student will use the SiN photonic waveguides to develop a novel on-chip technique to characterize bio-molecular interaction at sub-nanosecond time scale. In this proposed technique, the molecules are excited with a predetermined polarized light carried by the waveguide. The subsequent fluorescent emission is collected on chip by the slab waveguide and coupled out. The excitation and emission of fluorescence do not happen instantaneously. On average, the molecules stays at the excited state for a certain time before it emits the photon. During this fluorescent lifetime the molecular orientation changes. This causes a depolarization in the emission signal. The degree of depolarization in the emission can be used to probe the the weight and environment around the molecule. Hence,

the idea is to characterize the bio-molecular interaction at sub-nano-second time scale by quantifying the fluorescence depolarization due to the change in the molecular weight by the interactions.
The student will use FDTD simulations to optimize the optical design. Then (s)he will fabricate them using electron beam lithography. Finally, (s)he will experimentally validate the proposed technique. The student will gain hands-on experience with optical design, fabrication and experimentation. Sample preparation will be handled by the student in the imec III-V cleanroom in cooperation with the daily advisor. The candidate should have a strong interest in photonics and nanofabrication.

Type of project: Internship or thesis project or combination of both with a minimum duration of 1 year

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Materials Engineering, Mechanical Engineering, Physics, Computer Science

Responsible scientist(s):
For further information or for application, please contact Pieter Neutens (pieter.neutens@imec.be) and Pol Van Dorpe (pol.vandorpe@imec.be).

Nanoengineering for antibacterial applications

Antimicrobial resistance is an increasing threat to global public health since many conventional treatments become ineffective on bacteria which have developed a drug-tolerance. There's an urgent quest for new solutions to tackle this antibiotic resistance. In a recent discovery, it has been found that the nano-texturing on some insects' surface can effectively kill bacteria on contact. The bactericidal effects have been attributed to physical disruptions of cell walls caused by the nanostructures, and are independent of the chemical functionality. This discovery motivates a new approach to design and fabricate artificial antibacterial nano-materials.
The goal of this work is to engineer and optimize nanomaterials for antibacterial applications. imec's state-of-the-art CMOS technology platform enables fabrication of unprecedented ultra-dense nanopillar arrays with extremely precise control. In this work, you will employ a combined genetic and nano-engineering approach to further our understanding of mechanical bactericidal activity and devise new ways of improving the nanomaterial with higher efficiency.
Specifically, the following tasks are envisaged:

- Nano-engineering of materials to modify the topography profile, mechanical stiffness and surface chemistry by CVD, PVD, ALD, plasma etching and wet chemical etching etc.
- Material inspection and characterization by SEM, contact angle, FTIR etc.
- Study the effects of surface chemistry and surface morphology on bacterial attachment and colonization of nanostructured surfaces.
- Identify genetic factors contributing to sensitivity to killing by nanostructured surfaces through targeted mutagenesis and screening of genome-wide mutant libraries using viability staining and automated high-throughput fluorescence microscopy.

Type of project: Internship or thesis project or combination of both with a minimum duration of 4 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Materials Engineering, Bioscience Engineering, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact XiuMei Xu (xiumei@imec.be).

VI. Wearables

Capacitive measurement of non-ECG biopotentials

During the last two years imec has been working on the development of technologies for the unobtrusive acquisition of physiological signals from the human body. One of the techniques being used is the capacitive acquisition of biopotentials such as electrocardiography (ECG), bioimpedance (BIOZ), electroencephalography (EEG), among others. Although the idea of capacitive acquisition of biopotentials was initially mentioned in 1969 , the relatively recent developments of electronic technologies has made possible to implement such systems in a more practical way and with an increased signal quality, which has led to some commercial offerings of capacitive sensing devices. Despite these recent developments, most of the measurements are currently done in a laboratory setting with electrodes tightly strapped to the body, due to the characteristic sensitivity of capacitively acquired biopotentials to motion artifacts. Because of this, imec has focused not only on the development of systems for the capacitive acquisition of biopotentials, but also on their use in real-life environments through algorithms that optimally attempt to avoid and handle the motion artifacts making use of simultaneously acquired auxiliary signals.
Most of imec's activities in capacitive biopotential sensing have been related to the capacitive measurement of the electrocardiogram (ECG), which measures the electrical activity of the heart. Other biopotentials present on the body represent the electrical activity of other body functions: the electromyogram (EMG) represents muscle activity and the electro-encephalogram (EEG) represents a measure of brain activity. The proposed thesis topic concerns the study of the capacitive acquisition of biopotential signals other than ECG, notably EMG and EEG.
Within this thesis topic, the student will investigate the use of the existing capacitive measurement electronic systems for measuring these other biopotentials, possibly with modifications to the electronic circuits or the firmware and software. Regarding the EMG, the first step will be to define suitable measurement locations on the body which are useful for real-world applications. Then the student will build an experimental setup and experimentally verify the possibility of recording the EMG signals and validate the recorded signals against a reference wet gel electrode recording. Regarding the EEG, the student will continue a basic feasibility study to check whether it is possible to record EEG in a capacitive manner in a form factor which is compatible with real world applications. Based on the initial outcome of this study the focus of the remainder of the thesis will be put on either EMG or EEG recording.
The result of the thesis will be a report describing the performance and constraints of capacitive EMG and/or EEG recording together with recommendations on adaptations to the system required to improve the performance.
This thesis requires at least 5 months and preferably 6 months full-time work at imec headquarters in Belgium, with occasional trips to the imec office in Eindhoven, The Netherlands or other locations in Belgium or The Netherlands for which travel will be arranged when needed. This thesis work will be done under close guidance by the principal engineer (Tom Torfs) who is working in this domain.

Required skills: Test and measurement skills, mixed signal (analog and digital) electronic circuit knowledge, at least basic experience with embedded microcontroller firmware programming in C, at least basic experience using Matlab.

Type of project: Internship or thesis with internship project with minimum duration of 5 months

Degree: Master in Engineering Technology, Master in Science or Master in Engineering majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Tom Torfs (Tom.Torfs@imec.be) and Ivan Castro Miller (ivand.castro@imec.be).

Validation of capacitive cardiorespiratory measurement in real world studies

During the last two years imec has been working on the development of technologies for the unobtrusive acquisition of physiological signals from the human body. One of the techniques being used is the capacitive acquisition of biopotentials such as electrocardiography (ECG), bioimpedance (BIOZ), electroencephalography (EEG), among others. Although the idea of capacitive acquisition of biopotentials was initially mentioned in 1969 , the relatively recent developments of electronic technologies has made possible to implement such systems in a more practical way and with an increased signal quality, which has led to some commercial offerings of capacitive sensing devices. Despite these recent developments, most of the measurements are currently done in a laboratory setting with electrodes tightly strapped to the body, due to the characteristic sensitivity of capacitively acquired biopotentials to motion artifacts. Because of this, imec has focused not only on the development of systems for the capacitive acquisition of biopotentials, but also on their use in real-life environments through algorithms that optimally attempt to avoid and handle the motion artifacts making use of simultaneously acquired auxiliary signals.
The proposed thesis topic concerns the validation of the capacitive acquisition of the ECG (electrocardiogram) and respiration (using capacitive bioimpedance measurement) in real world applications.
The student will participate in the definition of the validation protocols and the execution of the measurements, collect the raw data of both the capacitive and the reference sensors, and acquire the signals into Matlab for comparison and validation. Also some practical work to integrate the recording systems into a workable validation setup and address any issues that may arise with the measurement hardware may be required.
Currently planned during the thesis is a sleep study on healthy volunteers (recording overnight in a real bed). In addition, a clinical study in hospital environment is planned after this work for which the student should participate in the definition of the measurement protocol based on the outcome of the sleep validation study.
The result of the thesis will be a report on the sleep study protocol and hardware/software setup and the raw signal validation, as well as recommendations for the clinical study protocol.
This thesis requires at least 5 months and preferably 6 months full-time work at imec headquarters in Belgium, with occasional trips to the imec office in Eindhoven, The Netherlands or other locations in Belgium or The Netherlands for which travel will be arranged when needed. This thesis work will be done under close guidance by the PhD researcher (Ivan Castro Miller) who is working in this domain.

Required skills: Test and measurement skills, experience using Matlab or a similar tool, at least basic mixed signal (analog and digital) electronic circuit knowledge, at least basic experience with embedded microcontroller firmware programming in C

Type of project: Internship or thesis with internship project with a minimum duration of 5 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Tom Torfs (Tom.Torfs@imec.be) and Ivan Castro Miller (ivand.castro@imec.be).

Motion artifact reference sensor study for capacitive and contact biopotential measurements

Imec has developed circuits and systems for measuring biopotentials such as electrocardiogram (ECG), electroencephalogram (EEG), bioimpedance (BIOZ), etc. from wearable devices, using either wet gel electrodes, dry contact electrodes or more recently using capacitive electrodes that do not need direct contact to the skin and hence can measure through textile.
Since such wearables are generally intended for ambulatory use (i.e. the person is moving around freely) the recorded signals tend to be distorted by motion artifacts, to varying degrees. The weaker the coupling of the electrodes to the body, the more severe the motion artifacts are: capacitive measurements suffer the most severely from motion artifacts, but also when using contact based electrodes motion artifacts remain a challenge for which methods for

improved robustness are highly desirable. One method imec wishes to apply is to record auxiliary sensor signals which can be used in algorithms to reduce the impact of the motion artifacts in the biopotential signal, e.g. through algorithms such as adaptive filtering. While some work has been done on using electrode-tissue impedance/capacitance or accelerometer/gyroscope data as reference signals for this, it is desired to study in more detail various possible reference signals and their potential for use in reducing motion artifacts.
The purpose of this thesis proposal is to build a prototype multisensor device which measures a variety of possible reference sensors (inertial, pressure/force, distance, ...) concurrently with the biopotential signal. This multisensor device will then need to be combined with imec's existing readout systems for contact biopotential as well as capacitive biopotential measurement. Signals will need to be experimentally recorded. The recorded signals will be used to study the correlations in motion artifacts between the reference signals and the biopotential signal, in order to permit the development of improved motion artifact reduction methods.
The result of the thesis will be the multisensor device design and prototype, the recorded signal dataset and a report describing the conclusions from the experimental recording regarding the observed correlations in the signals.
This thesis requires at least 5 months and preferably 6 months full-time work at imec headquarters in Belgium, with occasional trips to the imec office in Eindhoven, The Netherlands or other locations in Belgium or The Netherlands for which travel will be arranged when needed, as well as through teleconferences. This thesis work will be done under joint guidance by Tom Torfs of imec Belgium and Mario Konijnenburg of imec Eindhoven.

Required skills: Mixed signal (analog and digital) electronic circuit design, test and measurement skills, embedded microcontroller firmware programming in C, at least basic experience with signal processing in Matlab.

Type of project: Internship or thesis with internship project with a minimum duration of 5 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Tom Torfs (Tom.Torfs@imec.be) and Mario Konijnenburg (Mario.Konijnenburg@imec-nl.nl).

Reliable vital signs analysis with wearable sensors under ambulatory conditions

Device miniaturization and advancements in wireless sensor network (WSN) technology have enabled the development of wearable sensing devices which help towards continuous non-invasive physiological monitoring and analysis (heart rate, biometric identification etc.) in ambulatory/nomadic environments. Photoplethysmogram (PPG) and Electrocardiogram (ECG) are an important means of recording the physiological signals, reflecting the cardiac activity of human beings. However, the data collected in such nomadic environment presents a major challenge to obtain robust physiological parameters due to the presence of motion artifacts. Hence, it is quintessential to develop a strategy for collecting signals with high fidelity which could lead to robust signal analysis.
On this backdrop, there are two outlined research activities: 1) data collection from human subjects using wearable sensors (ECG, PPG, etc.) to prepare a physiological database for prospective analysis, 2) algorithmic evaluation on the collected data for artifact removal and de-noising. The algorithmic evaluation will primarily comprise of two main tasks: a) annotating the collected ECG data (which acts a reference for validating the information extracted from the PPG signal) using state-of-the-art algorithms (e.g. Pan Tompkin's algorithm) and b) exploring state-of-the-art noise removal and artifact reduction algorithms (e.g. Wavelet transform, Independent component analysis, etc.) for obtaining signal fidelity. These algorithmic explorations will set the platform for obtaining clean PPG signal which would help towards further physiological analysis (e.g. heart rate detection, disease classification, etc.).
As part of this exploration, a detailed experimental protocol including procedures, subjects, sensors and hands-on guidance on their use shall be provided along with adequate assistance towards algorithmic evaluation on the collected data.
Activities will specifically include:

- Data collection from human subjects
- Algorithmic evaluation – data annotation for acquired ECG signal
- Algorithmic evaluation – artifact removal

Type of project: Internship or thesis project with a duration of 6 to 9 months

Degree: Master in Engineering Technology and Master in Engineering majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Dwaipayan Biswas (Dwaipayan.Biswas@imec.be).

Channel-sharing design for high-density bio-signal recording applications

There is a general trend for biomedical applications to record ever more signals in parallel. A very concrete example is neural implants. These are very small probes that are implanted into the brain and record electrical activity form individual neurons. In order to increase the spatial resolution, state of that art neural probes proves hundreds of concurrent recording channels. This imposes a number of integration and scaling challenges.
The primary aim of this project is to study the feasibility of using channel-sharing techniques to address this challenge. The main research task would be to exploit frequency-division multiplexing in the analog domain. By merging multiple recording sites onto a single analog signal via frequency-division multiplexing, the hardware cost can potentially reduce significantly. However there are quite some challenges to solve, like understanding the right technique and place within the analog chain the implement it, how to efficiently resolve the original signals and quantify non-ideal effect like crosstalk, non-linear distortion effects and noise folding.
The project will involve intensive integrated circuit design and simulation activities. The candidate is expected to have solid knowledge in analog and mixed signal integrated circuit design, adequate experience of using cadence IC design software, strong interest in designing circuits for biomedical applications, and good potential of doing scientific research. The candidate will have access to imec's cutting edge IC design resources, and receive dedicated guidance from experienced researchers and IC designers.
The activities will include:

- State-of-the-art survey
- Conceptual design and simulation
- Analog front-end circuit design and simulation
- If time permits: custom ASIC layout and tapeout

Type of project: Thesis with internship project with a minimum duration of 6 months, but preferably 9 months

Degree: Master in Engineering majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Shiwei Wang (Shiwei.wang@imec.be).

Psychophysiological stress detection in a semi-controlled environment

Psychological stress is a worldwide growing problem. Currently the gold standard to measure stress is by using questionnaires. These are however just a snapshot, devious and subjective. To tackle this problem over the last years the focus of research has shifted towards physiological stress detection. Which is an objective measure, that can be monitored continuously. The goal is to measure stress by measuring physiological signals such as heart rate, skin conductance, temperature, etc. Research has already indicated that psychophysiological stress detection in a controlled environment, i.e. the laboratory, is possible. In an ambulant environment however, this remains a difficult task since multiple factors besides stress can influence physiology, e.g. physical activity. Therefore imec has collaborated in the past with a television program to collect physiological data in a semi-controlled environment. The dataset exists of heart rate signals and corresponding video images during the program. The goal is to link these heart rate signals with the participant's stress level. In this thesis work, first a scan of the state of the art (literature) on psychophysiological stress detection will be done. Then the aim is to first annotate the video images to identify

stressful and non-stressful periods per participant. Second a model should be developed that links these annotations with the measured heart rate.

Type of project: Internship project

Degree: Master in Engineering Technology and Master in Engineering majoring in Bioscience and Biomedical Engineering, Computer Science

Responsible scientist(s):
For further information or for application, please contact Walter De Raedt (deraedt@imec.be) and Elena Smets (elena.smets@imec.be).

Analysis and fusion of wearable sensor data

Microsystem technologies are currently stimulating the development and deployment of personal body area networks. These wireless networks provide lifestyle, assisted living, sports or entertainment functions for the user, without visible interference with their active lives. Prevention rather than detection and cure will be the future paradigm. In imec's Wearable Health program, such body area networks (BAN) with several different types of sensors are currently under development: ECG signals, skin conductance, ions in sweat, motion and many more signals can be monitored, recorded and wirelessly transmitted to a hub during longer periods of time. With the growing availability and acceptance of these sensor networks for improving our life quality, it is becomes attractive to use their information in a multitude of applications where the user can directly benefit from this information by managing his lifestyle and health. However combining information for several sensors can reveal new insights in different domains such as healthy behavior stimulation, assisted living, stress management.
Specific challenges are:

- Analyze cross platform sensor data (i.e. data from different types of sensors, such as a mix of commercial and research devices) simultaneously over large timeframes
- Search for correlations between data of these sensors (e.g. heart beat with skin conductance data for stressed people)
- Identify valid sensor data in long time series
- How to summarize the multitude of data in order to give a proper feedback message to the user?

In this thesis work, first a scan of the state of the art (literature) on sensor data management will be done. Furthermore, it is then the aim to elaborate a strategy for a flexible analysis and markup (data cleaning and correlation) tool for heterogeneous sensor data for use on a pc, a mobile device and in the cloud. In a first step, available captured data will be used to map sensor data from different sensors and correlate these data from different sensors: hearth rate, accelerometer data and skin conductance data will be studied over long time periods (days) searching for strategies to summarize extracted information in a clear and attractive way for the user. Next steps will then increase complexity by fusion of data from a more heterogeneous set of sensors.

Type of project: Internship or thesis project

Degree: Master in Engineering Technology and Master in Engineering majoring in Bioscience and Biomedical Engineering, Computer Science

Responsible scientist(s):
For further information or for application, please contact Walter De Raedt (deraedt@imec.be) and Elena Smets (elena.smets@imec.be).

VII. Photovoltaics

Advanced thin film solar cell architectures

The field of photovoltaics (PV) is composed of thin film (TF) and silicon (Si) solar cells, where TF solar cells have a rather simple cell structure, while the typical Si solar cell design is more complex as it is optically and electrically optimized. Standard TF solar cell devices are grown layer by layer on a rigid or flexible substrate. For example for copper indium gallium (di)sulfide or (di)selenide (Cu(In,Ga)(S,Se)2 = CIGS(e)) solar cells: First a molybdenum (Mo) rear contact is deposited, then the – typically 2.5 to 3.0 µm thick – CIGS(e) absorber layer, followed by a CdS buffer layer, and completed by an i-ZnO/ZnO:Al window layer. The typical Si solar cell design is more advanced, as it includes concepts to improve front and rear surface passivation, and optical confinement, as is the case for the passivated emitter and rear solar cell (PERC). The main reasons to introduce these advanced technologies is to reduce charge carrier recombination at the front and rear Si surfaces (by means of front and rear surface passivation layers) and increase optical confinement (by means of front texturing and highly reflective rear surface passivation layers), and consequently enhance the efficiency of ever thinner Si solar cells.
You will be part of a team that aims to revolutionize the design of CIGS(e) TF solar cells by implementing advanced surface techniques, introducing structures and layers also used in Si solar technology. This includes adding innovative reflective rear contacts to capture more light into the cell's active layers. Other new techniques envisaged are inversion layer emitters, passivated contacts and surface passivation layers. In combination, these new techniques should lead to cells with enhanced conversion efficiencies, and improved stability and reliability. This study of advanced TF solar cell architectures remains at the forefront of TF solar cell research, where physicists, engineers and chemists have the ability to successfully contribute. So, if you are interested in this work, then please contact the supervising scientist to find out if your profile fits this research.

Type of project: Internship or thesis project or combination of both with a minimum duration of 6 months

Degree: Master in Engineering Technology, Master in Engineering and Master in Science majoring in Chemistry/Chemical Engineering, Electrotechnics/Electrical Engineering, Energy, Materials Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Bart Vermang (Bart.Vermang@imec.be).

Novel carrier selective contacts for new concept silicon solar cells

Photovoltaic(PV) energy is getting more attention since it is clean and sustainable energy source. However, the levelized cost of energy(LCOE €/W) of PV energy has to be reduced to compete with other energy sources for expanding PV markets. To follow up those needs, many technologies are under investigation for higher efficiency, more cost effective process and new concept silicon solar cells.
imec is the top leading research institute in PV research field including next generation of PV technologies. Furthermore, many talented imec researcher and a state of art facility facilitate more rapid technological progress. A student will work as a part of the excellence during the internship.

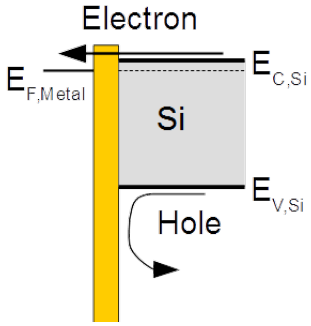


Figure 1. A Schematic concept of carrier selective contact. (A simple band diagram for electron contact.)

Internship student's research will focus on the contact of solar cells, especially on novel electron contacts which has low schottky barrier height and low carrier recombination at the contacts. The student will have to collect, combine and analyze information coming from materials, as well as structure of contacts. The student also has to use analysis methods to identify the back ground of the results of each specific cases. Quasi-Steady-State Photoconductance (QSSPC) lifetime measurement and J-V measurement will mainly be used to characterize the contact performance. At the end of the work, developed technologies will be integrated to the silicon solar cells.

Type of project: Internship project of 9 months - It is expected that the student presents his results in meetings, and writes high-quality reports at the conclusion of the internships (this can be a thesis).
This project is open to self-supporting students only (no imec allowance will be provided).

Degree: Master in Science and Master in Engineering majoring in material science, physics, electronics and any major related semiconductor technology

Responsible scientist(s):
For further information or for application, please contact Jinyoun Cho (jinyoun.cho@imec.be).

Measurement and demonstrators for innovative smart PV modules under non-uniform irradiation

It is well known that photovoltaic (PV) modules yield a lower energy in the field than what could be expected from their rated power, indicated as "peak-Watts (Wp)". This rating is determined, according to an industrially and internationally accepted standard, under "Standard Test Conditions (STC)". These conditions involve amongst others an irradiance of 1000 W/m2 ("AM1.5 spectrum"). Knowing that these values, in climates such as Belgium's, can only be maintained for longer periods of time on very sunny days with clear skies, it is clear that these conditions are relatively rare throughout the year and indeed the rated power effectively only indicates "peak" performance of the module.
In fact, the main energy yield losses (kWh/kWp), in particular in Belgium, can be attributed to a reduced illumination resulting in lower current and non-uniform illumination conditions (shading, clouds, soiling, ...) leading to current mismatch in the serially connected cells inside the module.
Therefore, in this topic, we want to measure the impact of such non-uniform and dynamic irradiation and shading conditions using an illumination setup for large-area (1x1.6m2) PV modules in order to more accurately evaluate panels in conditions that are closer to reality. Concretely, we want to be able to illuminate at lower irradiance levels, that can be applied with spatial non-uniformity and that can be varied in time. Apart from testing and characterizing the PV modules and (partly also) the setup itself, we want to use it to assess the performance of advanced "smart|" PV modules we are building|. They have configurable non-series topologies for which we want to evaluate the Eyield under many different shading conditions. We also want to finalize more of such configurable module demonstrators with specific topologies.

Measurements with this illumination setup and the demonstrator modules will then later on (outside the scope of this topic) be used to validate some complex optical-thermal-electrical models we are building to predict and evaluate the potential energy gain of future smart PV modules (WHAT-IF analysis).
The entire project will have a clear impact on relevant aspects of the future photo-voltaic energy landscape. It combines mostly practical skills with a more in-depth analysis of the obtained results. Considering the variety in challenges to be addressed within this topic (electronic hardware, control software, PV characterization, interpretation and extrapolation), it is important for us to have a candidate who already has a broad background in this domain. However, given that we work on this with a team, the specific focus of the MSc subgoals within the topic can be adapted to some extent to the interest of the applicant.

Type of project: Thesis project
This project is only open to self-supporting students (no imec allowance will be provided).

Degree: Master in Engineering majoring in Electrotechnics/Electrical Engineering, Energy

Responsible scientist(s):
For further information or for application, please contact Jonathan Govaerts (Jonathan.govaerts@imec.be) and Francky Catthoor (Francky.Catthoor@imec.be).

Modeling and measurement analysis of energy yield for advanced and smart PV modules

Photovoltaic (PV) solar panels provide a very attractive solution for future clean energy provision on-site. State-of-the-art, optimally installed PV modules preform excellent during clear-sky conditions. However, their energy yield reduces dramatically during non-steady state and installed at places which suffer from non-uniform illumination (e.g. static shading created by tree).
Imec is developing PV modules with additional or novel components to improve energy yield, especially during high-varying conditions and non-uniform illumination . First prove-of-concept modules are being installed and monitored to investigate the energy yield of these advanced and smart configurable PV modules. The electrical characteristics of PV modules depend on ambient conditions like ambient temperature, irradiance, wind speed and wind direction. Due to the highly varying character of these parameters, high frequency measurements are required in order to evaluate energy yield of the smart PV modules. Furthermore, more and more conventional PV systems are monitored nowadays. Both measurement campaigns creates an enormous stream of valuable information. In order to prove the benefits of additional components, or to detect faulty PV systems, we need to analyze this information.
The student will have to collect, combine and analyze information coming from both smart PV modules, as well as information from conventional PV systems. The student has to use this analysis to identify potential gains under each specific situation. If required, the student can perform additional (indoor or outdoor) measurements. Furthermore, the student will analyze energy yield of advanced and smart PV modules to improve existing electrical-thermal Eyield models. Also WHAT-IF explorations will be tried out with the resulting models.
The entire project will have a clear impact on relevant aspects of the future photo-voltaic energy landscape. It combines mostly practical skills with a more in-depth analysis of the obtained results. Considering the variety in challenges to be addressed within this topic (electronic hardware measurement, control software, PV characterization, modeling), it is important for us to have a candidate who already has a broad background in this domain. However, given that we work on this with a team, the specific focus of the MSc subgoals within the topic can be adapted to some extent to the interest of the applicant.

Type of project: Thesis or thesis with internship project
This project is only open to self-supporting students (no imec allowance will be provided).

Degree: Master in Engineering Technology and Master in Engineering majoring in Electrotechnics/Electrical Engineering, Energy

Responsible scientist(s):
For further information or for application, please contact Jonathan Govaerts (Jonathan.govaerts@imec.be), Francky Catthoor (Francky.Catthoor@imec.be) and Hans Goverde (Hans.goverde@imec.be).

Defining optimal conditions for perovskite thin film PV solar cell performance measurements

Perovskite thin film photovoltaic technology is currently the best 3rd generation PV candidate for commercialization. These materials have allowed for remarkable advances in efficiency of solution processed PV technology in less than a decade of research. However, commercial use of this technology still depends on advances in understanding of its stability and up-scalability. Imec's Thin film PV group is one of the groups pushing the knowledge boundaries of this technology, by showing possibilities of perovskite thin film PV technology at module level and its potential as a candidate for BIPV. To evaluate and fairly compare performance of this technology to other available PV technologies, conditions under which electrical measurements are performed are crucial. Current research shows that perovskite thin film PV is more peculiar in this regard to other currently available technologies. Defining all factors that affect perovskite performance and understanding their effects is the next step in assuring this technology can be sustainably applied. The focus of this work is to help investigate this aspect of perovskite thin film solar cells. The candidate has the opportunity to work in a highly motivating environment with cutting-edge technology thereby gaining a deep inside into the next generation of solar cells. The goal is to determine optimal conditions for an accurate measurement of the performance of perovskite solar cells.

Type of project: Thesis or internship with thesis project with a minimum duration of 6 months

Degree: Master in Science and Master in Engineering majoring in Electrotechnics/Electrical Engineering, Energy, Physics, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Lucija Rakocevic (Lucija.rakocevic@imec.be).

Wide-bandgap perovskite photovoltaics for high-efficient perovskite/silicon tandem solar cells

Developing high-efficiency, low-cost photovoltaics is the main goal of solar cell research today. The recent, rapid rise of perovskite photovoltaics has opened up an exciting route to surpass the efficiency limits of market-leading crystalline silicon (c-Si) solar cells. Perovskite/silicon tandem solar cells, a new class of photovoltaic devices, offer an attractive path to ensure long-term price reductions through high-efficiency photovoltaic modules. IMEC is at the forefront of research on such perovskite/silicon tandem solar cells. We have successfully developed perovskite/silicon tandem solar modules whose efficiencies are comparable to those of stand-alone c-Si solar cells. In order for the tandem solar cells to surpass the record efficiencies of silicon solar cells, development of an efficient wide-bandgap (> 1.6 eV) perovskite top solar cell is crucial. Existing wide-bandgap perovskites suffer from key issues that affect their performance. The aim of the project is to investigate and tackle the key performance issues, thereby enhancing the performance of wide-bandgap perovskite top solar cells, which in turn boost the efficiency of the tandem solar cell. We are looking for a candidate who is motivated to contribute to this multi-disciplinary domain. The candidate will benefit from the extensive knowledge and expertise of our team and work in a dynamic state-of-the-art research environment where physicists, chemists, and engineers collaborate efficiently.

Type of project: Thesis or internship project or combination of both

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Chemistry/Chemical Engineering, Energy, Materials Engineering, Physics, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Manoj Jaysankar (manoj.jaysankar@imec.be).

Boosting the wind effects for increasing the energy production of photovoltaic modules

It is well known that photovoltaic (PV) modules yield a lower energy in the field than what could be expected from their rated power, indicated as "peak-Watts (Wp)". This rating is determined, according to an industrially and internationally accepted standard, under "Standard Test Conditions (STC)". These conditions involve amongst others an irradiance of 1000 W/m2 ("AM1.5 spectrum"). Knowing that these values, in climates such as Belgium's, can only be maintained for longer periods of time on very sunny days with clear skies, it is clear that these conditions are relatively rare throughout the year and indeed the rated power effectively only indicates "peak" performance of the module. In fact, the main energy yield losses (kWh/kWp), in particular in Belgium, can be attributed to a reduced illumination resulting in lower current and non-uniform illumination conditions (shading, clouds, soiling, ...) leading to current mismatch in the serially connected cells inside the module. Next to that, the operation temperature is another element which is strongly affecting the energy production, as the conversion efficiency is reduced at elevated temperature. Therefore, to predict and optimize the energy yield of PV modules, a detailed and accurate understanding of the module's operating temperature required. Indoor and outdoor experiments have shown that the thermal behavior of PV modules is significantly influenced by wind effects. To gain insight into this effect, this master thesis focuses on investigating the effect of forced convection on the thermal response and hereby the electrical response of PV modules. Wind tunnel and outdoor setup measurements will be used to build and validate complex models which can be used to predict the thermal behavior of PV modules during any given condition. Finally, these models will be used to evaluate and optimize the energy gain of tomorrow's PV modules.

Type of project: Thesis project

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Computer Science, Physics, Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Hans Goverde (Hans.goverde@imec.be) and Eszter Voroshazi (Eszter.Voroshazi@imec.be).

Next generation PV module technologies

Photovoltaics panels around us are mainly (over 80%) based on c-Si solar cells, and this will continue to be the case for the foreseeable future. The module technology used for connecting and protecting these cells likewise has been established already long time ago. The currently standard module technology is based on stringing of cells for electrical interconnection and subsequent EVA lamination for encapsulation of these strings between a (transparent) front- and backsheet. This technology has proven its worth with operational lifetimes exceeding 20 years in harsh outdoor conditions. However it is time for change! Untapped potential of advanced materials and novel low-stress interconnection technologies integration in PV modules can bring a new era of innovation in traditional PV module fabrication. With this in mind, with its extensive expertise in cell technology, imec is starting to develop advanced module concepts. Several internship topics are proposed on the following subjects:

- Low-stress interconnection technologies are indispensable for the integration of thinner and more advanced cells in PV modules. We are investigating at imec unique concept suited both for traditional, bifacial and back contact solar cells using low temperature solder alloys. One of the first technical challenges is the selection of materials for reliable solder joints, their process integration and electrical and material testing with adhesion and interdiffusion studies..
- Simulation of the optical potential of novel materials in module design: First relying on an open-access simulation tool the advantage of new materials should be quantified. Both to provide input and validate the modelling

dedicated samples, small laminates will be prepared and characterized. Limitation of the existing simulation tools might be overcome by defining own simulation framework.

- Reliability investigation of novel encapsulation materials in combination of traditional and novel cell types. Relevance of currently used accelerated reliability tests should be validated by first monitoring the performance loss of samples under different stress conditions and comparing with samples exposed to operational conditions. In parallel the impact of novel stress conditions and/or sequence of stress tests will be explored. Finally, understanding the root-cause of the failure in the different conditions will be critical part of the investigation.

These topics are multi-disciplinary in nature, as they look both at the technology for PV module fabrication (with limited size), as well as the materials and opto-electrical characterization and operation aspects of those modules. The focus can be adapted to some extent to the interest and capabilities of the applicant. Most of the work will be done in the state-of-the-art device processing lab of imec. The student will receive a broad training on full device processing and characterization tools. After a short training period it is expected that the student can work independently and focusing on his/her investigation.

Type of project: Internship project

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Physics, Materials Engineering, Electrotechnics/Electrical Engineering, Energy

Responsible scientist(s):
For further information or for application, please contact Jonathan Govaerts (Jonathan.govaerts@imec.be), Tom Borgers (Tom.borgers@imec.be) and Eszter Voroshazi (Eszter.Voroshazi@imec.be).

Enhancing the energy production of photovoltaic module by advanced and novel concepts

Photovoltaic (PV) solar panels provide a very attractive solution for future clean energy provision on-site. State-of-the-art, optimally installed PV modules preform excellent during clear-sky conditions. However, their energy yield reduces dramatically during non-steady state and installed at places which suffer from non-uniform illumination (e.g. static shading created by tree). IMEC is developing PV modules with additional or novel components and novel cell technologies to improve the energy yield, especially during high-varying conditions and non-uniform illumination. First prove-of-concept modules are being installed and monitored to investigate the energy yield of these advanced and smart configurable PV modules. The electrical characteristics of PV modules depend on ambient conditions like ambient temperature, irradiance, wind speed and wind direction. Due to the highly varying character of these parameters, high frequency measurements are required in order to evaluate energy yield of the smart PV modules. Furthermore, more and more conventional PV systems are monitored nowadays. Both measurement campaigns creates an enormous stream of valuable information. In order to prove the benefits of additional components, or to detect faulty PV systems, we need to analyze this information. The student will have to measure collect, combine and analyze information coming from both smart PV modules, as well as information from conventional PV systems. The student has to use this analysis to identify potential gains under each specific situation. If required, the student will perform additional (indoor or outdoor) measurements and design and manufacture new experiments. Furthermore, the student will analyze energy yield of advanced and smart PV modules to improve existing electrical-thermal E-yield models. Also WHAT-IF explorations will be tried out with the resulting models. The entire project will have a clear impact on relevant aspects of the future photo-voltaic energy landscape. It combines mostly practical skills with a more in-depth analysis of the obtained results. Considering the variety in challenges to be addressed within this topic (electronic hardware measurement, control software, PV characterization, modeling).

Type of project: Thesis project

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Physics, Electrotechnics/Electrical Engineering, Computer Science

Responsible scientist(s):

For further information or for application, please contact Hans Goverde (Hans.goverde@imec.be) and Eszter Voroshazi (Eszter.Voroshazi@imec.be).

Silicon heterojunction (HJ) interdigitated back-contacted (IBC) solar

As a world-leading R&D hub, imec aspires for radical innovation that maximizes societal impact by creating smart sustainable solutions that enhance life. Photovoltaics (PV) is one among a wide range of focus areas of imec. This internship/master's thesis proposal is in the PV department, focused on the advancement of the silicon heterojunction (HJ) interdigitated back contacted (IBC) cell technology, which has garnered plenty of attention in recent years.
HJ-IBC cells are the most efficient silicon solar cells in the world, with Kaneka breaking the world record efficiency recently with its remarkable 26.33% cell. Imec is one of the institutes involved in the development of this cell technology. Hydrogenated amorphous silicon (a higher band-gap material) is deposited on crystalline silicon to form the heterojunction and also to passivate the silicon surface. This unique combination allows high efficiencies to be attained, compared to regular homo-junction silicon solar cells. In addition, to maximize light absorption, an all-back contacted solar cell architecture is used.
Another important trend in PV is the reduction in silicon wafer thickness. At thicknesses well below 100 µm, processing of HJ-IBC cells on thin silicon after bonding them to the module glass becomes an interesting approach that is being advocated by imec in its i2-module concept. This approach comes with a variety of interesting challenges.
The focus of this internship is the development of processes that would enable the improvement of the cell efficiencies while simplifying the process sequence. Due to the nature of the topic, there is plenty of scope to learn and acquire knowledge and skills in a wide variety of topics that would stand the student in good stead in his/her future endeavors. The student will work and interact with a team of experts, and the results will be followed up closely. At the same time it is expected that the student takes initiative and is able to work independently and enthusiastically, once the initial training period is finished.

Type of project: Internship project with a duration of 9 months
It is expected that the student presents his results in meetings, and writes high-quality reports at the conclusion of the internships (this can be a thesis).

Degree: Master in Science and Master in Engineering majoring in Material Science, Physics, Electrotechnics/Electrical Engineering, Chemistry/Chemical Engineering

Responsible scientist(s):
For further information or for application, please contact Hariharsudan Sivaramakrishnan Radhakrishnan (Hariharsudan.Sivaramakrishnan@imec.be).

Integration of silicon heterojunction solar cells

Imec performs world-leading research in nanoelectronics. Together with its partners, Imec applies its scientific knowledge in ICT, healthcare and energy. In a unique high-tech environment, international top-talented people work to contribute to a better life in a sustainable society. The current proposal for an internship or Master's thesis is about making better solar cells.
For the making of the recent world record solar cells (25.6%, 26.3%), the manufacturers used the deposition of hydrogenated amorphous silicon. This is because amorphous silicon has some beneficial intrinsic material properties. Moreover, it is deposited at low temperatures (<200°C) which brings about unique possibilities for solar cell fabrication. At the same time, to reach high efficiencies a good understanding of the different fabrications steps is needed.
The focus of this internship is the deposition of amorphous silicon layers, and their integration into silicon heterojunction solar cells. The student will work and interact with a team of experts, and the results will be followed up closely. At the same time it is expected that the student takes initiative and is able to work independently once the initial training period has finished.

Type of project: Internship project with a duration of 9 months
It is expected that the student presents his results in meetings, and writes high-quality reports at the conclusion of the internships (this can be a thesis).

Degree: Master in Science and Master in Engineering majoring in Material Science, Physics, Electrotechnics/Electrical Engineering, Chemistry

Responsible scientist(s):
For further information or for application, please contact Twan Bearda (twan.bearda@imec.be).

VIII. GaN Power Electronics

There are currently no Master thesis/internship projects available in this research domain.

IX. Sensor Solutions for IoT

There are currently no Master thesis/internship projects available in this research domain.

X. Wireless IoT Communication

IOT Demonstrator

You will:

- Create an IOT demonstrator combining different wireless communication techniques and different sensors (Lora, Sigfox, BTLE, NBIOT, LTE,...)
- Study the positive and negative points of each technique such as power consumption, data rate, localization possibilities, ease of use, ...
- Create a basic library (schematics, layout and firmware) for jump starting future developments for SME
- Create a platform to allow SME to perform field tests before deciding on a particular implementation

The IOT Demonstrator would combine academic research on the different communication techniques, practical implementation with the focus on schematic entry, layout, firmware development, test application development and field testing. The student would experience a complete electronic development cycle with the aid of experienced imec employees and would gain significant knowledge on the different IOT communication and localization possibilities. During the development, product reliability and manufacturability will be key aspects to be monitored.

Type of project: Thesis project

Degree: Master majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Boris Leekens (Boris.leekens@imec.be) and Geert Willems (Geert.Willems@imec.be).

Low-power phase detector for AM-PM predistortion in mm-wave digital transmitters

For wireless communications, millimeter wave solutions are raising a lot of interest in the research environment. The large available bandwidth of several GHz at those frequencies promises a large capacity for high-throughput applications. Advanced CMOS technology is now capable of enabling radio transceivers operating at mmwave frequencies. This opens the way to deploy mmwave CMOS transceivers for applications where low cost and volume production are key.
Analog transmitters are less suitable for integration in advanced CMOS nodes. Digital transmitters are more compact and more robust to transistor imperfections and mismatches compared to analog transmitters, but they typically fall short with respect to high-end performance requirements such as out-of-band noise and spurious emission.
AM-PM (analog modulation to phase modulation) pre-distortion in digital transmitters is important to achieve the performance and speed required by future wireless communication applications.
In this research project on chip phase detectors for AM-PM predistortion in mm-wave digital transmitters will be investigated and a suited solution implemented in downscaled CMOS. The detector will have to consume limited power and must have negligible loading effect on the Power amplifier in the transmitter.

Type of project: Thesis or internship project or combination of both with a minimum duration of 6 months

Degree: Master in Engineering majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Khaled Khalaf (Khaled.Khalaf@imec.be).

High-speed DAC for future radar and mmwave sensing applications

The demand for inexpensive and ubiquitous accurate motion-detection sensors for road safety, smart homes and robotics justifies the interest in single-chip mm-Wave radars: a high carrier frequency allows for a high angular resolution in a compact multi-antenna system and a wide bandwidth allows fora high depth resolution. With the objective of single-chip radar systems, CMOS is the natural candidate to replace SiGe as a leading technology. Radar solutions in advanced CMOS technology offer a path to lower power, more compactness and higher levels of integration. Moreover, at the expected high manufacturing volumes, CMOS technology is intrinsically lower cost. Radar systems have to handle challenges such as spillover (signal leaking from the transmitter to the receiver) . This spillover causes false targets to be detected. To compensate for this spillover a high speed / high resolution ADC (analog to digital conversion circuit) and DAC (digital to analog conversion circuit) circuit have to be integrated in the system to handle the high dynamic range requirements. In this research project a 8bit, 4Gsps DAC will be investigated and designed.

Type of project: Thesis or internship project or combination of both with a minimum duration of 6 months

Degree: Master in Engineering majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Jan Craninckx (Jan.Craninckx@imec.be).

Exploration of millimeter wave hybrid analog-digital architecture with realistic RF modeling

For wireless communications, millimeter wave solutions are raising a lot of interest in the research environment thanks to advanced CMOS technology being now capable of operating at these frequencies. The large available bandwidth of several GHz at those frequencies promises a large capacity for high-throughput applications. To compensate the high propagation losses in millimeter wave bands, multiple antennas can be implemented to provide the benefit of antenna array gain. Moreover, digital beamforming increasing the link budget can be combined with multiple antenna solutions (MIMO) offering more benefits to the system such as increased capacity by sending multiple streams in parallel. More recently, the idea of very large multiple-antenna systems (Massive MIMO) has come as a way to reduce the power consumption and provide even more capacity. However, MIMO and Massive MIMO require many analog front-ends to support full digital beamforming which is a challenge at millimeter wave due to prohibitive cost, complexity, and high power consumption. The shift of MIMO/Massive MIMO to millimeter wave is not straightforward and for this reason hybrid analog-digital architectures have been proposed. Early results indicate that merging Massive MIMO and millimeter wave technologies would be possible using a limited number of analog front-ends. However, these results are still at early stage and they require an in depth analysis as they do not guarantee the efficacy of hybrid analog-digital architectures under realistic RF impairments. The implementation at millimeter wave induces several critical RF non-idealities that must be addressed during the system design. Phase noise and carrier frequency offset arising from local oscillators cause a particular challenge when distributing the signals to the many antennas. On top of that, hybrid architectures requires particular attention to the power losses introduced using power splitters and power combiners when targeting high energy efficiency, as well as and mismatches introduced by phase shifters between the different streams. In its 5G program, imec has developed a complete simulation environment that simulates transmitter, propagation at millimeter wave, and receivers. This simulator is very flexible and supports phased arrays, MIMO configuration, analog and RF non-idealities. The goal of this thesis is to adapt the imec simulator to support RF non idealities for hybrid architectures and use it to investigate different solutions guaranteeing a sufficient performance under realistic conditions.
The work will include:

- Literature survey
- Implementation of RF impairments based on existing models
- Evaluation of performances and study of the impact of non-idealities
- Development of compensation techniques

Required profile: The successful candidate will have to show a strong understanding of wireless communications, radio transceivers and signal processing. Proficiency with Matlab is a must.

Type of project: Thesis or internship project or combination of both with a minimum duration of 6 months

Degree: Master in Engineering majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Steve Blandino (steve.blandino@imec.be).

XI. Radar Sensing Systems

There are currently no Master thesis/internship projects available in this research domain.

XII. Solid State Batteries

Conformal deposition of Li-ion conductors for 3D thin-film batteries

Lithium-ion batteries (LIB) with a solid-state electrolyte can potentially solve two key limitations of today's LIB with liquid electrolytes, namely, safety issues due to the flammability of the electrolyte and cycle life time due to unwanted side-reactions at the solid/liquid interface. The improved safety and potentially extended lifetime of solid-state LIBs makes them highly desired, however, finding a solid-state electrolyte with Li-ion conductivity comparable to existing liquid electrolytes (>1mS/cm) that also exhibits good electrochemical stability is an extremely difficult task. Utilization of a solid-state composite electrolyte (SCE) is one promising concept for solving these challenges. Through design on the nanoscale, an SCE with enhanced Li-ion conductivities can be obtained by exploiting the highly conductive interface existing between a Li-salt and an oxide such as alumina and silica. This thesis project focuses on the development of SCE based on a thin-film platform with the emphasis on interface control and functionalization, both through gas-phase deposition and nanocasting, in order to obtain the optimal Li-ion conductivity. The experimental work of the project is carried out at imec facilities. Next to the fully equipped battery lab and thin-film deposition facilities, the imec state-of-the-art nanofabrication and characterization facilities will be available to carry out the research. Novel methods of conformal growth of thin inorganic-organic hybrid films using a combination of atomic layer deposition (ALD) and molecular layer deposition (MLD) techniques form the basis of the project work. Next to process optimization and physical characterization, large effort goes into the electrical and electrochemical characterization of the individual thin films and half-cell stacks (battery electrode/electrolyte). The main goal is to explore thin films as solid electrolytes for 3D thin-film lithium-ion batteries.

Type of project: Thesis project

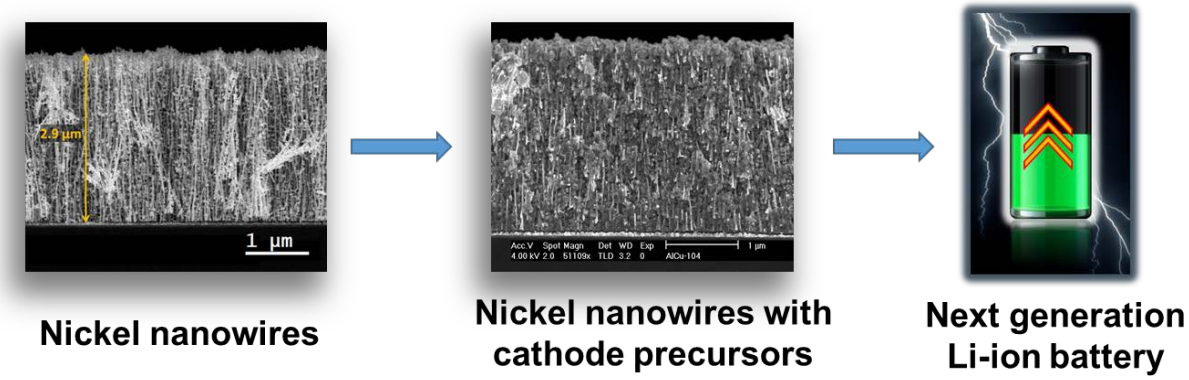
Degree: Master in Science and Master in Engineering majoring in Bioscience Engineering, Chemistry/Chemical Engineering, Materials Engineering, Electrotechnics/Electrical Engineering, Physics

Responsible scientist(s):
For further information or for application, please contact Knut Gandrud (Knut.Bjarne.Gandrud@imec.be).

Synthesis and characterization of cathode active materials for next-generation nano-engineered lithium-ion batteries

One of the current activities of imec's Energy Storage group is the development of next-generation fast charging lithium ion batteries based on nickel nanowires current collector architectures. Due to significantly increased surface area of the nanowires, when plated with thin layers of electrode active materials, these batteries should allow for much shorter charging times, as compared with classical batteries. These batteries are designed to power small portable devices such as mobile phones, smart body sensors, or digital eyewear. Since the nanowire battery is designed taking into account economical factors, the fabrication is done using simple, upscallable and cheap electrochemical methods. The electrodeposition of cathode materials yields electrochemically inactive layers (called cathode precursors), which need to be activated by thermal reaction with lithium precursors. However, certain nanoscale thermodynamic factors limit the compatibility of nickel nanowires for thermal treatments with some precursors, causing failure of the devices.
In this master thesis, synthesis and characterization of various, nanowires-compatible cathode active materials will be performed. Among the cathode material candidates are various lithium insertion compounds such as $LiCoO_2$ or $LiNiO_2$ [1]. The investigated cathode materials will be electrochemically deposited onto the nickel surface, converted to their active form and characterized. Attention will be put on determination of conditions suitable for conversion of the cathode precursors and its role on cathodes performance. The work will provide the Master researcher hands-on experience of the electrochemical synthesis of energy storage materials, together with various characterization techniques such as cyclic voltammetry, TGA/DSC or GI-XRD. Some of the operations will be

performed in controlled innert atmosphere inside of a glovebox. The project provides opportunity to work in a multinational team of scientists and engineers in a mixed scientific-industrial environment.
The student should have sufficient knowledge of physical and inorganic chemistry.



[1] N. Nitta, F. Wu, J. T. Lee, G. Yushin, Materials Today, vol. 18 (2015), p. 252-264

Type of project: Thesis project or combination of thesis with internship with a minimum duration of 6 months

Degree: Master majoring in Bioscience Engineering, Chemistry/Chemical Engineering, Materials Engineering, Nanoscience & Nanotechnology

Responsible scientist(s):
For further information or for application, please contact Stanislaw Zankowski (Stanislaw.zankowski@imec.be).

Solid-state thin-film batteries

The introduction of the rechargeable Li-ion battery in 1991 brought about a general revolution in the battery landscape. As a result of its high energy density, more energy could be stored in a small volume, which meant that the energy needed to power a device such as a laptop could be made portable. The emergence of this battery also enabled the rapid rise of smart, mobile electronics and is today also introduced in electric vehicles and home storage applications. To generate current, both electrons and lithium ions move from the negative to the positive electrodes. During charging, they move in the opposite direction. The amount of electrode material mainly determines the storage capacity. The electrolyte provides the ionic conductance between the electrodes and defines the power of the battery. The liquid electrolytes which are used today pose safety and health risks due their flammable and corrosive nature. Therefore all solid-state batteries are being explored. The solid-state design lends itself also to completely new battery architectures, such as the compact 3D thin-film battery. In this type of battery, the thin-film stack is coated over a micro-structured substrate instead of on a planar substrate. This method enables very thin films to be used for the electrode and the electrolyte, while achieving energy densities comparable with current-day battery technology. However, the actual capacity will still be limited due to the intrinsically small dimensions of these batteries. For this reason it is important that this battery can be recharged quickly so that the microsystem is never without power. This is made possible by using thin films of at most a few hundred nanometers thick. As a result, the ions only need to travel a short distance and the battery can be recharged in a matter of minutes. These small form batteries are intended for microsystems such as implants, sensors and ‘smart cards’. In this master thesis, you will explore novel deposition techniques and investigate their mechanism. The obtained electrode and electrolyte thin-film stacks will be characterized for their battery performance.

Type of project: Thesis project

Degree: Master in Science and Master in Engineering majoring in Bioscience Engineering, Materials Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Philippe Vereecken (Philippe.Vereecken@imec.be).

XIII. Data Science and Data Security

There are currently no Master thesis/internship projects available in this research domain.

XIV. Neuroelectronic Research (NERF)

Introduction

Imec, VIB (Flanders' leading life science institute), and the Leuven University have set up a joint basic research initiative to unravel the neuronal circuitry of the human brain: Neuroelectronics Research Flanders (NERF). Supported by the Flemish Government, NERF looks into fundamental neuroscientific questions through collaborative, interdisciplinary research combining nanoelectronics with neurobiology. It intends to push the boundaries of science, by zooming in on the working of neurons at an unprecedented level of detail. In the long run, NERF will generate new insights in the functional mapping of the brain, as well as research methodologies and technologies for medical applications, i.e. diagnostics and treatment of disorders of the central and peripheral nervous system. The NERF labs are located at the imec premises. Read more: http://www.nerf.be/.

Novel device for fluidic interfacing with the brain

The enormous burden brain disorders pose on affected individuals and health care systems worldwide, calls for new ways to prevent, treat and cure brain disorders like Alzheimer's, schizophrenia, autism, and epilepsy. In order to obtain mechanistic insights into brain function in basic and translational research as well as for drug discovery, physical interfacing with the brain in vivo for measurement and manipulation purposes is essential. From a therapeutic perspective, direct fluid delivery to the brain is advantageous since it can limit potential side effects of systemic administration and enables therapeutic use of substances, which normally do not cross the blood brain barrier.
We have previously developed the design for a novel fluidic interfacing device, which addresses current technical limitations. In this master thesis, we will realize and test the first prototype of the device. This multidisciplinary project at the interface of biology and engineering will provide fundamental insights into the biology and biophysics of the brain. The project capitalizes on the unique combination of skills and expertise available at Neuroelectronics Research Flanders (NERF) and its founding partners. If successful, our novel approach will become a key enabling technology for obtaining a more mechanistic understanding of the brain in preclinical animal models and it will lead the way towards novel treatments for brain disorders in the clinic.
The project includes the following project phases:

1. Fabrication of prototype
2. Basic testing & characterisation in vitro
3. Testing & characterisation in vivo
4. Extend proof-of-concept experiments towards pre-clinical applications

Type of project: Internship or thesis project or combination of both with a minimum duration of 3 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Bioscience Engineering, Electrotechnics/Electrical Engineering, Mechanical Engineering

Responsible scientist(s):
For further information or for application, please contact Sebastian Haesler (Sebastian.Haesler@nerf.be) and Luis Hoffman (Luis.Hoffmann@nerf.be).

Unraveling neuronal activity during locomotion

Plasticity in sensorimotor circuits is the basis of motor learning during development and after central nervous system trauma. Spinal cord injury disintegrates functional sensorimotor ensembles by disconnecting circuits below lesion from the rest of the nervous system. While an incomplete lesion is often associated with partial functional recovery, our lack of knowledge of the genetic identity, precise anatomical connectivity, and function of the participating circuit components poses a great challenge to understand and intervene in the process of motor recovery.
Using flexible electrode technology available at imec, the aim of the project is to reveal neuronal activity of non-injured and injured spinal cord circuits in real-time during walking in a neuronal population specific manner in an unprecedented resolution. In this project we will use combined methods of mouse genetic engineering and viral technologies to identify neuronal populations involved in a given locomotor task with phase-specific temporal precision. Interns/students' responsibilities will include implementation of surgical technique for stimulation/recording electrodes, behavioral training, kinematic recording and analyses as well as briding between collaborating technology teams and the Takeoka lab's neuroscience circuit expertise.

Type of project: Internship or thesis project or combination of both with a minimum duration of 6 months

Degree: Master in Science and Master in Engineering majoring in Bioscience Engineering, Computer Science, Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Aya Takeoka (Aya.takeoka@nerf.be).

Engineering new devices and tools to study how the brain processes and stores information

Advancing our understanding of how the brain performs computations and supports cognition, requires sophisticated tools and devices for experimental read-out and manipulation of neural activity. In the Kloosterman laboratory at the Neuro-Electronics Research Flanders (NERF, www.nerf.be), we are interested in revealing the mechanistic principles of information processing and storage in the brain's memory system. For this, we develop and apply advanced brain implants and other tools for experimental neuroscience that enable large-scale monitoring of neural activity in animals that perform complex behavioural tasks. Examples include flexible neural probes integrated in 3D-printed arrays, implantable mini-microscopes and devices for automated behavioural control.
We are looking for highly motivated candidates with a background in Electrical Engineering, Mechanical Engineering or similar background, who would like to contribute to the design, fabrication and testing of new tools that advance experimental neuroscience. Candidates will work in the NERF laboratories on the imec campus, in an international, multi-disciplinary and stimulating research environment. Candidates need to be familiar with one or more of: electronics design, 3D CAD design, robotics & micro-controller platforms and programming (C++/Python). The ideal candidate is able to work pro-actively and independently in a small team of dedicated neuroscientists.

Type of project: Internship or thesis project or combination of both with a minimum duration of 6 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Computer Science, Electrotechnics/Electrical Engineering, Mechanical Engineering, Nanoscience & Nanotechnology, Physics

Responsible scientist(s):
For further information or for application, please contact Fabian Kloosterman (fabian.kloosterman@nerf.be).

Understanding memory through real-time processing and closed-loop manipulation of brain activity

The human brain is the most complex biological machine with over 80 billion active cells and a thousand times more interconnections between the cells. The Kloosterman laboratory at Neuro-Electronics Research Flanders (NERF, www.nerf.be) is interested in understanding how the brain learns about the world and how it uses this information for future benefit. For this, we probe the brain's memory system using large-scale measurements of electrical activity during the acquisition of memory tasks and subsequent sleep. These measurements provide a rich view on patterns of brain activity that mediate remembering, planning and decision making. We apply advanced data analysis approaches to interpret the relation between brain activity and behaviour. To further reveal the causal role of specific activity patterns in cognition, we have developed novel algorithms and a custom software platform for real-time signal processing and closed-loop perturbations.
We are looking for highly motivated candidates who would like to advance our understanding of brain function in an international, multi-disciplinary and stimulating research environment. The candidates will work on the development of software tools for real-time processing of streaming experimental data and/or offline analysis of complex data sets. Candidates should have demonstrated programming experience (C++ and/or Python) and be familiar with digital signal processing, machine learning and/or neuro-statistics. The work will take place at the NERF laboratories on the imec campus. The candidates are expected to work pro-actively and independently within a small team of dedicated neuroscientists.

Type of project: Internship or thesis project or combination of both with a minimum duration of 6 months

Degree: Master in Engineering Technology, Master in Science and Master in Engineering majoring in Computer Science, Electrotechnics/Electrical Engineering, Physics

Responsible scientist(s):
For further information or for application, please contact Fabian Kloosterman (fabian.kloosterman@nerf.be).

Using machine learning and deep neural networks to automatically identify components of neural circuits in the visual system

The shape and position of a neuron conveys critical information about its identity and function. The identification of cell types from structure is a classic method that relies on the time-consuming and labour intensive tracing of its structure. Recent advances in experimental and imaging techniques now allow the acquiring of data sets approation for data-driven approaches to neuronal circuit analysis feasible, with the caveat automated image processing pipelines become a necessity. Recent advances in deep neural networks and machine learning techniques have demonstrated the power of these techniques to reliably perform automated image recognition online. This work has begun to be translated to work in laboratory environments. The goal of this project is to apply/develop these techniques to a set of imaging data where we would like to automatically identify to neuronal components at the very beginning of two neural circuits known to drive freezing and escape behaviors. The suitable student should already be familiar with machine learning and imaging processing techniques, as well as have good knowledge of at least one programming language (preferably Julia, Python, MATLAB or C++).

Type of project: Internship or thesis project or combination of both with a minimum duration of 6 months

Degree: Master in Science and Master in Engineering majoring in Bioscience Engineering, Computer Science, Electrotechnics/Electrical Engineering, Physics

Responsible scientist(s):
For further information or for application, please contact Karl Farrow (karl.farrow@nerf.be).

Using virtual reality to study the function and neural circuits in the mouse visual system

The main aim of the lab is to understand the fundamental principals underlying the function of neural circuits during behavior. Towards this goal we investigate how sensory information is processed along the neural pathways that generate visually guided behavior. The lab uses two-photon calcium imaging, high-density probe recordings, optogenetics and computer based analytical methods of neural activity in awake behaving animals. Using these techniques, we study the activity of genetically defined neural populations in response to visual stimulation and perturb components of these circuits to understand their function in visual processing and visually guided behavior. Ultimately, the experiments are designed to understand the fundamental principles of sensory information processing in the brain. The visiting students are expected to have a decent background in computer programming and instrumentation. Together With the visiting student we will aim to build and use a virtual reality system that will allow us to record neural activity while the animal performs visually guided tasks, i.e. plays a video game. These experiments will allow us to investigate the processing of visual information with and without sensory feedback.

Type of project: Thesis project or combination of thesis with internship

Degree: Master in Science and Master in Engineering majoring in Physics, Bioscience Engineering, Computer Science, Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Karl Farrow (karl.farrow@nerf.be).

XV. Microelectronics Design

Structured ASIC development for space applications

In this project the student will investigate application of structured ASIC as a cost-effective solution for high performance, low volume radiation hardened ASICs.
For more than 15 years imec IC-link develops, in cooperation with the European Space Agency (ESA), a radiation tolerant digital standard cell library and full custom IP, in 180 nm CMOS. These building blocks are used in IC's used by the space industry. Because high energetic radiation, existing outside the earth's atmosphere, is able to influence the operation of standard CMOS chips, there is a need for high quality radiation tolerant electronics; several general measures are added to a standard CMOS design flow to accomplish this.
Scaling of CMOS technology is done to increase the performance per watt and decrease the cost per transistor but it has also the effect that the set-up costs increase with a major contributor the cost of the masks that contain the layout to be printed on the wafer. When thinking about using 28nm technology for space application these set-up costs may limit the application area of the technology and at the same time keep the improved performance out of reach for space applications.
One of the solutions to the set-up costs is the use of FPGA where these costs are distributed over all the FPGAs but where each of them can be programmed with a custom design. In order to provide the customizability a trade-off is made in the performance area. An intermediate solution are so-called structured ASICs. These build on the sea-of-gate technique used on older technologies. This technique combines a non-custom array of transistors with customized interconnect layers to derive an application specific chip. With technology scaling the number of interconnect layers has also increased meaning that having a fully customized interconnect stack bear high set-up costs. The structured ASIC technique then only uses a reduced set of custom metal and/or via masks to come to a more optimized trade-off between set-up cost and performance. Another option impacting the cost is the possible use of multi-layer masks (MLM) where up to four metal layer or four via layers can be combined on one mask leading to lower set-up costs but higher per transistor cost.
The tasks for this master thesis are then:

- Investigate and study existing structured ASICs offerings
- Design radiation hardened basic building block for a structured ASIC
- Investigate cost-performance trade-off using different number of customized layers and taken into account the possibility of using MLM.
- Briefly indicate requirements on the place&route flow.

To perform this master thesis the student has at imec access to state-of-art electronic design automation (EDA) tools from Cadence, Mentor and Synopsys going from process and transistor level simulation, to full-custom design environments to digital implementation flows. Depending on the direction taken during the investigation and development of this project the right tool for the job will be decided under guidance of the design experts at imec. In order to provide support during design main part of this thesis needs to happen on-site in imec. The student should have basic knowledge of micro-electronics design and digital circuits.

Type of project: Internship or thesis project

Degree: Master in Science majoring in Electrotechnics/Electrical Engineering

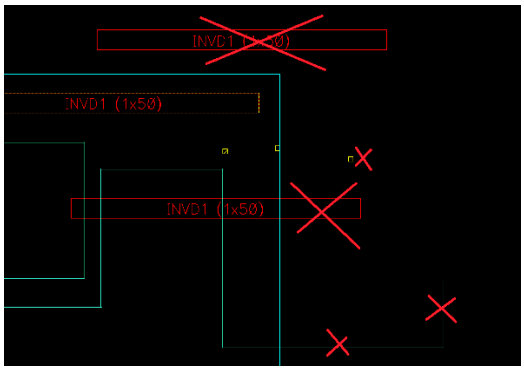
Responsible scientist(s):
For further information or for application, please contact Staf Verhaegen (Staf.Verhaegen@imec.be) and Geert Thys (Geert.Thys@imec.be).

Implementation of analog layout improvements

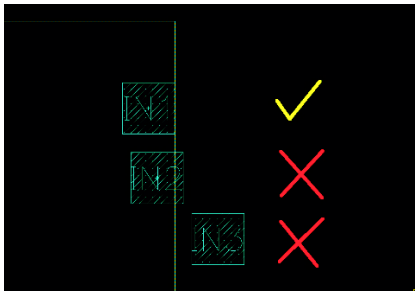
The purpose of the internship is to improve the general quality of the (analog) layouts. These improvements will be done through additional checks on top of classical ERC, RAD, ANT, DRC and LVS verifications. These extra checks

will help the layout engineer in their layout analyses. It will be necessary to keep in mind that these extra checks will have to be portable between different CMOS technologies (e.g. 180nm, 65nm, ..) CMOS, but also between different foundries (e.g. UMC, TSMC, Silterra, ..) ... and also advanced technologies (FFET).
The work will start with a study of the analog layout tools, verifications tools, deck, Skill coding and PDK. Some examples of checks to implement are listed below. An exhaustive list will be compiled once the internship starts.

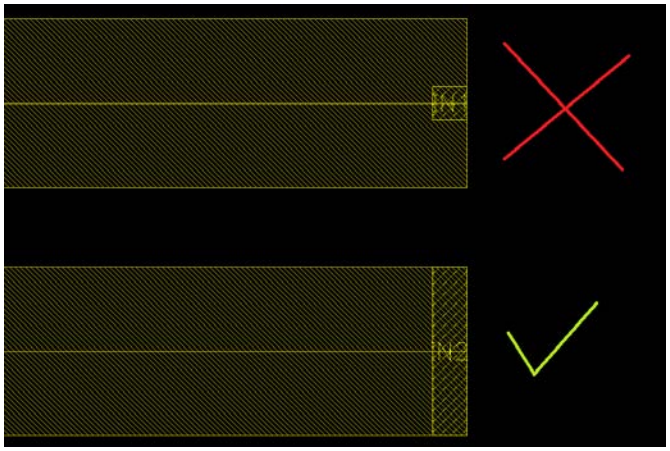
- Check to see if the PR Boundary encloses all elements



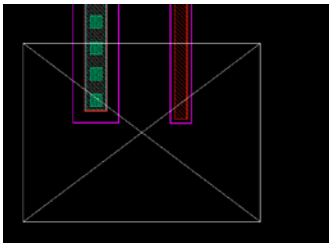
- Check to see if all pins are on the PR boundary



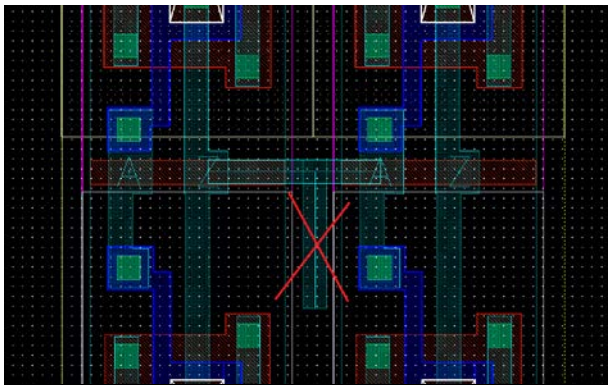
- Check to see if the width of the pin are equivalent at the metal



- Flag if the substrate contact cannot cross the border between separate grounds



- Flag all dangles and floating metal



This work requires the student to be present at imec facilities on a regular basis.
Software used:

- Cadence Virtuoso layout (Environment L,XL & GXL)
- Mentor Calibre (layout verification)

- Linux OS

Time allocation:

- 35% study "Layout training & verification tools, DECK, Skill coding, PDK"
- 30% R&D
- 35% implementation in the PDK

Type of project: Internship project

Degree: Master in Engineering Technology majoring in Electrotechnics/Electrical Engineering, Computer Science

Responsible scientist(s):
For further information or for application, please contact Stephane Zagrocki (Stephane.Zagrocki@imec.be) and Geert Thys (Geert.Thys@imec.be).

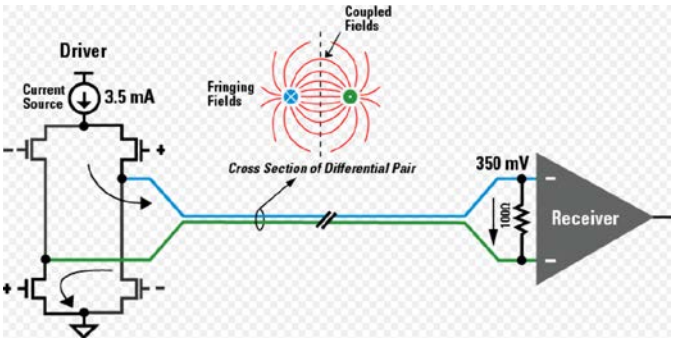
Development of RadHard LVDS IP in 65nm CMOS

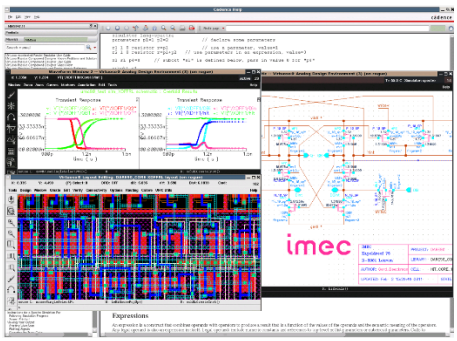
The purpose of the work is to add fail-safe functionality to already existing LVDS receiver cell. This requirement prevents the receiver from switching on noise in the absence of an input signal. For operation in space this is an essential requirement as it protects the system to physical fault conditions.
For more than 15 years imec IC-link develops, in cooperation with the European Space Agency (ESA), a radiation-tolerant digital standard-cell library and full-custom IP, in 180 nm CMOS. These building blocks are used in IC's used by the space industry. Because high-energetic radiation, existing outside the earth's atmosphere, is able to influence the operation of standard CMOS chips, there is a need for high-quality radiation-tolerant electronics; several general measures are added to a standard CMOS design flow to accomplish this.
LVDS stands for Low Voltage Differential Signaling, and is an electrical standard for high speed digital communication at system level. The electronics implementing this standard is essentially analog.
Currently we are starting to set up a new eco system based on 65 nm CMOS, and the design of LVDS IP is part of this work. Cells as existing in 180 nm can serve as a reference, but by no means can circuits just be copied. Also, extra features are to be added: cold spare functionality and SET robustness. Cold spare has to do with the use of a system as a cold redundant unit. SET (Single Event Transient) robustness refers to the impact of energetic particles.
The work is to start with a study of some literature (introduction to LVDS, and to requirements for space electronics). Then design is to be done: transistor-level schematics are made, which are simulated (spice). When all requirements are validated, the cell has to be layed-out: a "mask design" is to be made, which serves as the input for the IC foundry (located in Taiwan) to produce the silicon.
In order to go through the whole specification-to-layout flow, state-of-the-art software is used. This requires the student to be present at imec on a regular basis. Software used:

- Cadence Virtuoso (schema & layout), Analog Design Environment XL & Spectre (simulation)
- Mentor Calibre (layout verification)
- Linux OS

Time allocation:

- 20% studying literature
- 50% design & simulation
- 30% layout





Type of project: Internship or thesis project

Degree: Master in Science majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for applicatIon, please contact Jan Wouters (Jan.Wouters@imec.be) and Geert Thys (Geert.Thys@imec.be).

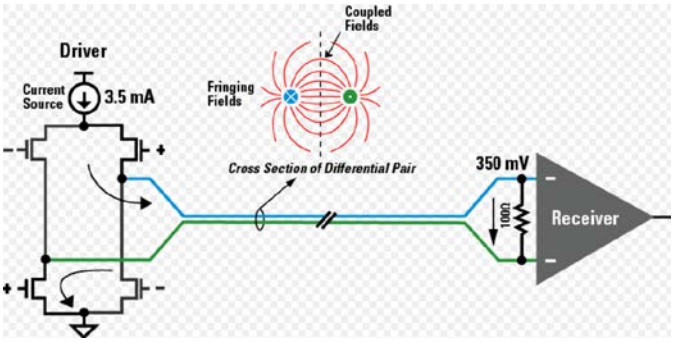
Improvements to RadHard LVDS IP in 180nm CMOS

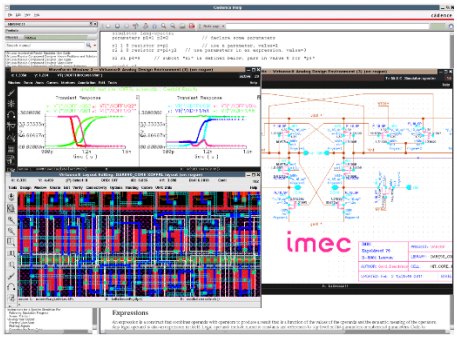
The purpose of this work is to add fail-safe and cold spare functionality to existing LVDS receiver and transmitter cells. Fail-safe prevents the receiver from switching on noise in the absence of an input signal, while cold spare provides redundancy at system level. For operation in space these are essential properties as it protects the system from physical fault conditions. SET (single event transient) robustness is another important requirement in the harsh space environment.
For more than 15 years imec IC-link develops, in cooperation with the European Space Agency (ESA), a radiation-tolerant digital standard-cell library and full-custom IP, in 180 nm CMOS. These building blocks are used in IC's used by the space industry. Because high-energetic radiation, existing outside the earth's atmosphere, is able to influence the operation of standard CMOS chips, there is a need for high-quality radiation-tolerant electronics; several general measures are added to a standard CMOS design flow to accomplish this.
LVDS stands for Low Voltage Differential Signaling, and is an electrical standard for high speed digital communication at system level. The electronics implementing this standard is essentially analog. The fail-safe function attempts to drive the output of the data receiver to a known state under floating or disconnected input conditions, this is when no valid input signal is present. Without this function, the cell output might oscillate in response to input differential noise. Several schemes exist that use external resistors. However, the idea is to only use on-chip active (transistor) circuits (active fail-safe) to realize the requirement; essentially a window comparator is to be implemented.
The work is to start with a study of some literature (introduction to LVDS, and to requirements for space electronics). Then design is to be done: transistor-level schematics are made, which are simulated (spice). When all requirements are validated, the cell has to be layed-out: a "mask design" is to be made, which serves as the input for the IC foundry (located in Taiwan) to produce the silicon.
In order to go through the whole specification-to-layout flow, state-of-the-art software is used. This requires the student to be present at imec on a regular basis. Software used:

- Cadence Virtuoso (schema & layout), Analog Design Environment XL & Spectre (simulation)
- Mentor Calibre (layout verification)
- Linux OS

Time allocation:

- 20% studying literature
- 50% design & simulation
- 30% layout





Type of project: Internship or thesis project

Degree: Master in Science majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Jan Wouters (Jan.Wouters@imec.be) and Geert Thys (Geert.Thys@imec.be).

Single event transient test vehicle: characterization of a 65nm CMOS technology against heavy ions

For more than 15 years, imec IC-link has developed, in cooperation with the European Space Agency (ESA), a radiation-tolerant digital standard-cell library and full-custom IP in 180 nm CMOS. These building blocks are often an integral part of IC's used by the space industry. Because high-energy radiation, existing outside the earth's atmosphere, is able to influence the operation of standard CMOS chips, there is a need for high-quality radiation-tolerant electronics. Several general measures are therefore added to a standard CMOS design flow to accomplish this remedial design approach.
A chip designed for space applications, like communication satellite, needs to be hardened against heavy ion strikes. Indeed, in deep space there is no atmosphere to filter the heavy ions rejected by astral corps (star, super nova...). When a heavy ion hits a p- or an n-silicon area, it creates an electron-hole pair. In the presence of an electrical field, such as at the drain of a MOS transistor, part of the electron-hole pair created is not recombined and so creates a transient current pulse.
The integral of this current can reach a charge of the order of 1pC (1pC on a capacitor of 1pF would cause a 1V drop on the capacitor!). It is important that first, this charge does not destroy the device (through latch up for instance); and secondly, does not lead to a malfunction of the chip. Some design techniques may be used to make the chip "immune" to single event transients (transient faults due to a heavy ion strike).
To use this hardening design technique efficiently, it is important to have an accurate electrical model of the heavy ion (see figure 2). The best way to reach this target is to directly measure the effect of the heavy ion on elementary structure (single transistor, elementary digital gate...).
The first part of this thesis would entail the design of a circuit to be placed around the elementary cells to capture the single event transient (SET). This circuitry will detect any SET on the elementary device and its duration, thanks to a fast delay line (see figure 1). With these two pieces of information, we can construct an accurate electrical model of the heavy ion based on the double exponential (see figure 2).
The second part of the thesis will be focus on the layout of the cell designed in the first part. After the completion of the layout the student will simulate the chip with its parasitic (extracted from the layout) to verify that the SET capture circuitry is still fast enough.
In order to go through the whole specification-to-layout flow, state-of-the-art software is used. This requires the student to be present onsite at imec on a regular basis.

Software used:

- Cadence Virtuoso (schematic & layout), Analog Design Environment XL & Spectre (simulation)
- Mentor Calibre (layout verification)
- Linux OS

Time allocation:

- 20% studying literature
- 50% design & simulation
- 30% layout

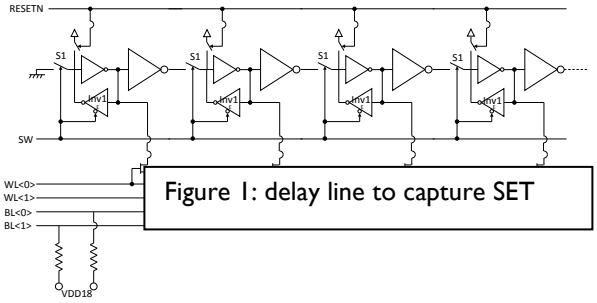


Figure 1: delay line to capture SET

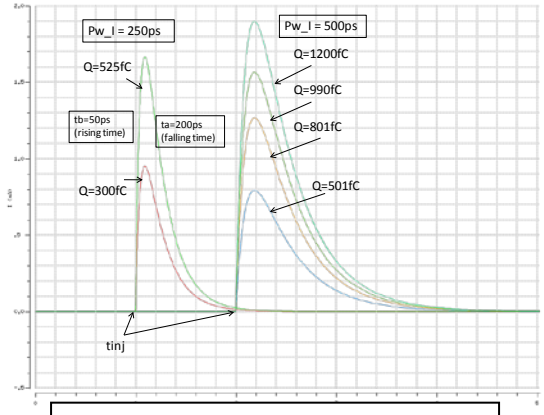


Figure 2: heavy ion electrical representation

Type of project: Internship or thesis project

Degree: Master in Science majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Laurent Berti (laurent.berti.ext@imec.be) and Geert Thys (Geert.Thys@imec.be).

Design of a clock phase extraction circuit for a high speed serial link

For more than 15 years imec IC-link has developed, in cooperation with the European Space Agency (ESA), a radiation-tolerant digital standard-cell library and full-custom IP, in 180 nm CMOS. These building blocks are often an integral part of IC's used by the space industry. Because high-energy radiation, existing outside the earth's atmosphere, is able to influence the operation of standard CMOS chips, there is a need for high-quality radiation-tolerant electronics. Several general measures are therefore added to a standard CMOS design flow to accomplish this remedial design approach. Additionally, IC-link supports other IMEC research departments to industrialize/promote their innovations.
The purpose of this thesis/internship is to design a clock phase acquisition for a high speed serial link (1Gb/s). The data and the clock signal will be transmitted to the chip through a LVDS interface. The phase shift between the data channel and the clock will be strongly dependent on the PCB design (and thus a priori unknown). Thus, the clock signal must be properly delayed to sample the data at the optimum time (see figure 1). This delay must be stable across temperature and supply levels (to calibrate the delay only at the initialization of the link).
The first part of this thesis will entail the design and layout of a high speed LVDS receiver and secondly to design and layout a programmable delay that is constant over the temperature and the supply level.

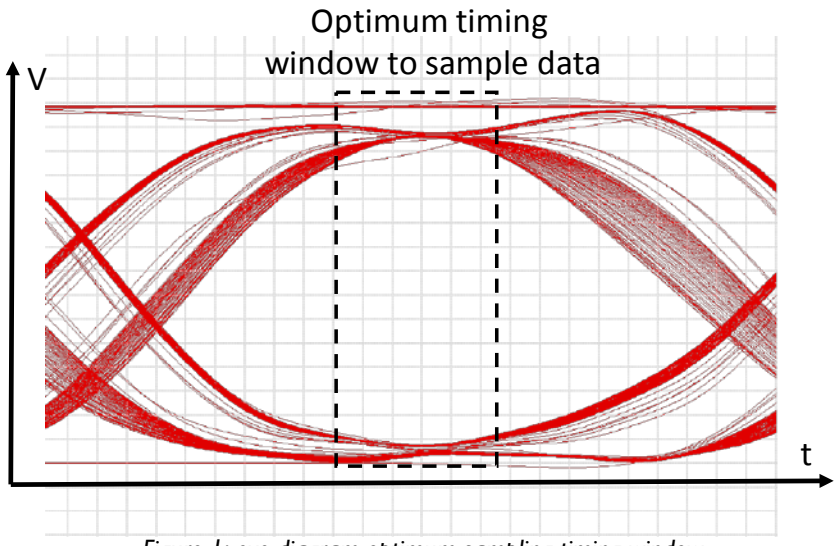


Figure 1: eye diagram optimum sampling timing window

In order to go through the whole specification-to-layout flow, state-of-the-art software is used. This requires the student to be present onsite at imec on a regular basis.
Software used:

- Cadence Virtuoso (schema & layout), Analog Design Environment XL & Spectre (simulation)
- Mentor Calibre (layout verification)
- Linux OS

Time allocation:

- 20% studying literature
- 50% design & simulation
- 30% layout

Type of project: Internship or thesis project

Degree: Master in Science majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Laurent Berti (laurent.berti.ext@imec.be) and Geert Thys (Geert.Thys@imec.be).

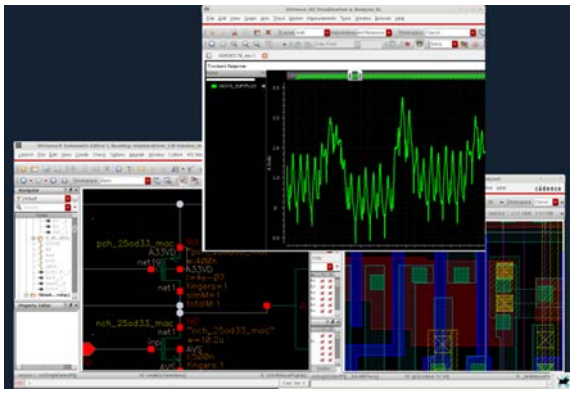
Design of RadHard Flip Flop with Razor technique

In this master thesis the student will be made familiar with radiation hardened design and applied to the design of a radiation hard D-flip-flop. The target of the master thesis is to combine the mitigation of transient radiation induced effect using the Razor technique with the existing design of bit-flip radiation hardened latches and flip-flops.
For more than 15 years imec IC-link develops, in cooperation with the European Space Agency (ESA), a radiation-tolerant digital standard-cell library and full-custom IP, in 180 nm CMOS. These building blocks are used in IC's used by the space industry. Because high-energetic radiation, existing outside the earth's atmosphere, is able to influence the operation of standard CMOS chips, there is a need for high-quality radiation-tolerant electronics; several general measures are added to a standard CMOS design flow to accomplish this.

The Razor technique1 was developed to in situ detect timing errors to allow dynamic voltage and frequency scaling without the need of worst-case margins or parallel representative measurement circuits. The principle is to detect a change on the input of a flip-flop after the value has been latched. A second clock signal that is delayed from the main clock signal is used for that purpose. In the Razor II paper2 it was shown that this technique can be used to detect and mitigate transient radiation effects.
For the 65nm standard cell library under development at imec a design is available that is setup hardened e.g. bit-flips caused by radiation are prevented. The target of this master thesis is to combine this design with the design of the Razor flip-flop. As the detection of timing errors is not a target of the standard cell library it has to be investigated if using this fact timing and area of the flip-flop can be optimized. Using the resulting flip-flop will impact the digital design flow using them so guide lines should be provided on using the flip-flop in such a flow. The breadth of this effort van be adapted to the time and expertise present for this project.
The summary of the task is then the following:
Study the design of the Razor flip-flop and the setup radiation hardened flip-flop.

- Combine the designs in one to reach a bit-flip and transient radiation hardened flip-flop.
- Layout and optimize the design and layout of the flip-flop taking into account the fact no timing error detection will be performed with the flip-flop.
- Provide guide lines for usage of the flip-flop in a digital design flow. The breadth of this task will be adapted to the time and expertise available for this master thesis.

To perform this task a state-of-the-art design environment is available at imec using EDA software from Cadence and Mentor as illustrated in picture below. To provide support main part of design has to happen on site at imec.



(1) S. Das, D. Roberts, S. Lee, S. Pant et al., "A Self-Tuning DVS ProcessorUsing Delay-Error Detection and Correction," IEEE J. Solid-State Circuits, vol. 41, no. 4, Apr. 2006
(2) D. Blaauw, S. Kalaiselvan, K. Lai, W.-H. Ma, S. Pant, C. Tokunaga, S. Das, D. Bull, "Razor II: In Situ Error Detection and Correction for PVT and SER Tolerance", ISSCC 2008

Type of project: Internship or thesis project

Degree: Master in Science majoring in Electrotechnics/Electrical Engineering

Responsible scientist(s):
For further information or for application, please contact Staf Verhaegen (Staf.Verhaegen@imec.be) and Geert Thys (Geert.Thys@imec.be).

Automation and improvement of custom EDA flow

In the full-custom design team of IC-link a custom EDA (electronic design automation) flow is used for designing circuits. This flow is mainly Linux based using several tools like shell and python scripting, makefiles, trac ticketing system and specific EDA tools each with their own scripting languages.
Several steps in this flow are now still manual and ripe for automation, also some continuous integration like improvements so designers can get automatic feedback on design changes performed. For this internship no specific knowledge on chip design is needed. The student needs to be able to understand the requirements of the engineers using the flow and in cooperation with them propose and implement more automation and continuous feedback.
The student should implement this in the best tool for the job and thus be flexible in this selection.

Type of project: Internship project

Degree: Master in Engineering Technology and Master in Science majoring Computer Science

Responsible scientist(s):
For further information or for application, please contact Staf Verhaegen (Staf.Verhaegen@imec.be) and Geert Thys (Geert.Thys@imec.be).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