Master Thesis & Internship Projects @ imec

2018 Topic Guide

Information

Students from universities and engineering schools can apply for a Master thesis and/or internship project at imec. Imec offers topics in engineering (technology) and sciences in different fields of research.

All Master internship and thesis projects currently available at imec are collected in this topic guide. The projects are classified according to the imec expertises. You can find more detailed information on each expertise on www.imec-int.com. In addition, in this catalogue you will find the projects available with imec.IC-link and NERF (www.nerf.be)

How to apply?

Send an application email including your motivation letter and detailed resume to the responsible scientist(s) mentioned at the bottom of the topic description you choose.
The researcher(s) will screen your application and let you know whether or not you are selected for a project at imec.
It is not recommended to apply for more than three topics.

There is no application deadline. We accept applications at any time and deal with them throughout the year.

Master internship students usually receive an allowance. However, some research groups only accept self-supporting students. Do you want to know upfront whether the project you wish to apply for provides financial support? When sending in your application email then check the remuneration details with the responsible scientist. For some projects, it is already mentioned in the project description that an allowance will not be provided.

For more information, go to the Master thesis & internship section on the Work at imec tab on www.imec.be. Do you have additional questions, then send an email to student@imec.be.

For Master thesis/internship projects in **imec the Netherlands** refer to
http://www.holstcentre.com/careers/thesis-opportunities or contact talent@imec-nl.nl.

After acceptance

In case of acceptance to our internship program you are bound to embark on a very exciting and interesting experience! For imec, your contribution as a student will be essential in meeting the deliverables in our programs. Therefore, it is vital that - once you accept to come to imec - we can count on your commitment and dedication for the entire duration of the internship period.

I. CMOS & beyond CMOS

Machine learning based computational lithography

As the chip scaling continues with the technology nodes to follow Moore's law, computational jobs such as optical proximity correction (OPC) and design-for-manufacturability (DFM) have become too intensive to carry out with introduction of more design data and models (mask, optical, resist, etch, topography-aware and CMP) to improve chip printability and prediction accuracy. 'Big Data' usually refers to data volumes that are so large that traditional data processing applications are inadequate, which exactly represents current OPC and DFM confront. In consequence, increased risk with increased ramp-up time from the research to the high volume manufacturing has been pointed out as risk. The student will use Machine Learning to apply the learning into computational lithography field that includes OPC and DFM. The student will learn conventional OPC and DFM flow, and work toward R&D in application of Machine learning into OPC and DFM flow with goals of 1) development of new algorithm, 2) reduction in number of computational iteration, and 3) optimization/minimization of DOE to shorten turn-around-time (TAT) in Semiconductor manufacturing. Machine learning and optimization may include study of a. Pattern recognition, b. Pattern extraction, c. Classification in Machine learning Modeling. Optimization incorporates mathematical and statistical concepts (effect, global/local min. search algorithm), or a new concept.

Type of project: Internship or thesis project, or combination of both

Duration: 6 months

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in computer science, electrotechnics/electrical engineering, nanoscience & nanotechnology, physics

Responsible scientist(s):
For further information or for application, please contact Ryan ryoung-han kim (Ryan.ryoung.han.kim@imec.be) and Jae Uk Lee (Jae.uk.lee@imec.be).

Ferroelectric device electrical characterization

Ferroelectric hafnium oxide (HfO2) attracted a lot of interests since its discovery in 2007. Its scalability and CMOS compatibility are two advantages over conventional ferroelectric materials, favoring new device integration. Such material could enable the fabrication of low power devices in standalone semiconductor manufacturing facilities due to its scalability and CMOS compatibility. Already, a one-transistor ferroelectric field effect transistor embedded NVM has been implemented for low power application. This integration demonstrates the potential utilization of such material system for memory applications. Doped ferroelectric HfO2 Metal/Insulator/Metal capacitors have been widely studied for DRAM and FeFET applications. Silicon electrodes have not been discussed in much detail so far, though it provides an input for vertical ferroelectric FET (V-FeFET), based on Flash NAND architecture.
The existence of ferroelectric properties in HfO2 was discovered in 2007 by Böscke et al. using silicon as dopant in a planar Metal/Insulator/Metal (MIM) capacitor. The presence of a small amount of dopant, a capping layer and a thermal anneal facilitate the transformation of the monoclinic phase into a non-centrosymmetric orthorhombic phase which is the origin of this property. FE-HfO2 has been mainly studied with planar MIM capacitor. The use of polycrystalline silicon (poly-Si) as electrodes has been proposed for the first time by IMEC. Such study provides an important input for 3D applications, aiming at disrupting 3D NAND market.
As an intern in memory device team at imec, you will support state-of-the-art ferroelectric technology development by characterizing and understanding of semiconductor devices. During your internship, you will have the opportunity to work with device characterization, reliability and integration engineers. You will be challenged by working on a cutting-edge technology, aiming at an innovative device never reported before in literature.
Successful candidates must have:

- Excellent communication skills, both oral and written
- Ability to independently adapt & learn with the outcome of a completed project
- Background in solid state physics and semiconductor processing
- Constitute a plus but not a requirement:
- Device characterization experience
- Experience in the operation and of semiconductor instrumentation including, but not limited to:
    - Parameter analyzers, SPA, SMU
    - LCR meters
    - Oscilloscopes
    - Pulse & waveform generators
    - Wafer probers
- Knowledgeable in a variety of software tools and operating systems, including but not limited to:
    - Python
    - C/C++
    - Unix/Linux
    - Matlab/Octave

Type of work: 80% ferroelectric electrical characterization, 15% understanding, 5% literature

Type of project: Internship or thesis project

Duration: 6–9 months

Degree: Master majoring in electrotechnics/electrical engineering, physics, materials engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Simone Lavizzari (simone.lavizzari@imec.be) and Jan Van Houdt (Jan.VanHoudt@imec.be).

Selective low-k dielectric growth using metal nitride conversion approach

Developing next generation chips for logic computation remains based on dimensional scaling. However, at present we entered an era where scaling is not anymore applied to basic functional elements (transistor, interconnect circuitry) but to the logic cell as a whole. New cell geometries are investigated in order to gain space by compacting all logic elements closer each to the other. In this framework, self-aligned architectures using selective deposition concepts are essential building blocks. The principle of selective deposition is to be able to grow a few nanometers thick film (1 to 10nm) on some specific locations of the substrate, and not on others. This is typically done using sacrificial passivants or blocking agents (self-assembled monolayers – SAMs) or doing specific surface treatments (plasma-based) to de-activate or activate specific areas of the substrate. Depending on the natures of the substrate and the selectively deposited films, one consider four challenges: metal-on-metal deposition (MoM), dielectric-on-metal deposition (DoM), metal-on-dielectric deposition (MoD) or dielectric-on-dielectric deposition (DoD). DoD is particularly challenging since the targeted dielectric constant (k-value) is below 3, which poses significant challenges for the composition and microstructure of the grown/deposited dielectric, which added to the selectivity requirements, make the overall deposition process challenging. In this work, we will focus on DoD. Instead of doing direct deposition of a low-k dielectric, we propose an alternative two-step scheme. In the first part, a high-k dielectric (metal nitride) is deposited, using a conventional Atomic Layer Deposition (ALD) method. In the second part, this high-k is converted to a low-k carbo-nitride, using high-T chemistry in controlled atmosphere. The goal of the internship/Ms work is to understand the details of this high-T conversion reaction as a function of temperature, nature of gaseous reactants, pressure in the conversion chamber, starting metal-nitride composition and thickness (linked to diffusion lengths for in-diffusion and out-diffusion of species). Criteria of evaluation will be : final thickness of formed low-k dielectric, roughness, dielectric constant, composition, chemical resistance. The selectivity of the conversion process will be checked towards metals relevant to the most advanced technology nodes (Cu, Ru). Once

a viable conversion process will be established, some patterned vehicle will be used, where the selective conversion will be tested on a substrate showing both dielectric and metallic surfaces. The student will be trained on relevant ovens and etch systems (300mm, 200mm, LAB depending on availability), on material characterization techniques such as spectroscopic ellipsometry, grazing-angle Fourier-transformed X-ray spectroscopy, X-ray reflection spectroscopy, atomic force microscopy, scanning electron microscopy, and will interface with the Materials Characterization & Analysis (MCA) group of imec for more complex physico-chemical characterization techniques (XPS, SIMS, RBS). The k-value extraction will be done using available techniques at imec (metal-dots for small samples and/or Hg probe for 300mm wafers). The student's activity will be embedded and be reported into a module meeting devoted to self-aligned deposition techniques.

Type of project: Internship or thesis project

Degree: Master in Science majoring in chemistry/chemical engineering, physics, materials engineering

Responsible scientist(s):
For further information or for application, please contact Jean-Francois de Marneffe (Jean-Francois.deMarneffe@imec.be).

Impact of thermal budget on spin-orbit torque and SOT-MRAM performances

There is considerable interest in electrically controlling nano-magnets in order to develop non-volatile magnetic memories (MRAM) [1]. The microelectronics industry is facing major challenges related to the volatility of CMOS cache memory elements (usually SRAM and eDRAM). Due to decreasing devices size, leakage current in standby mode are now dominating the power dissipation of CMOS circuits. Furthermore, the increased density and reduction in die area lead to heat dissipation and reliability issues. Integration of non-volatility in memory hierarchy would solve these issues by incredibly minimizing static power consumption. MRAMs are among most credible candidates that are low power and fast enough to compete with SRAM and replace them at cache level. Most advanced MRAM devices are magnetic tunnel junctions (MTJ) that consist of two ferromagnetic layers separated by a very thin oxide barrier, one of the layer being the storage layer, the other is used as reference layer. Depending on the relative orientation of the magnetization of these two layers (parallel/ anti-parallel), the MTJ cell will exhibit low/high resistance through the tunnel magneto-resistance effect (TMR), defining the reading state (0/1). The writing operation relies on either the Spin Transfer Torque (STT) [1], the transfer of spin angular momentum from the reference layer to the free layer, or the Spin-Orbit Torque (SOT) [2,3], due to the charge-spin conversion mediated by the spin-orbit interaction. The SOT mechanism allows for decoupling the read and write operations using a novel 3-terminal geometry (figure 1.a), enabling for robust deterministic magnetization reversal at sub-ns scale [4]. This project explores materials and devices for SOT-MRAM applications and aims at characterizing the impact of thermal annealing on SOT-MRAM stacks performances.
This work is part of the exploratory magnetic memory project of imec. It covers competences in the fundamentals of magnetism and spintronics as well as in the structural, magnetic, and transport properties of thin film materials. Below are the main task to be performed during this internship. It will mostly consist of magnetic and electrical characterization (60%), nano-fabrication (30%) and literature (10%).

1. Characterization of the magnetic properties of trilayer stacks and full SOT-MTJ stacks as a function of annealing temperature for different SOT systems.
2. Fabrication of simplified SOT devices (using above tri-layers) in order to analyze the impact of thermal annealing on SOT amplitude and critical switching current density.
3. Characterization of 300mm integrated SOT-MTJ cells (figure 1) as a function of annealing temperature.

[1] C. Chappert et al., Nature Material (2007), [2] M. Miron et al., Nature (2011); [3] K. Garello et al., Nature Nanotech (2013); [4] K. Garello et al., Appl. Phys. Lett. (2014)

Type of project: Thesis or thesis with internship project

Duration: 6 months

Degree: Master in Engineering majoring in physics, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Kevin Garello (Kevin.garello@imec.be).

Low temperature epitaxial growth of Ga doped SiGe for future device applications

Current downscaling of MOS devices goes together with modifications of the transistor device geometry, the implementation of new materials and the introduction of new device concepts. Planar devices have been replaced by FinFET structures and new designs such as Gate All Around FETs (GAA) are being considered to tackle future scaling issues. In parallel, Si has successfully been replaced by strained SiGe (or strained Ge) in high mobility channels as well as for the implementation of Source/Drain (S/D) stressors. The reduction in transistors' dimensions leads to a reduction in the S/D contact area and an increase in contact resistance, which limits device performance. New approaches are therefore required to significantly reduce contact resistance. This triggered the research community to assess the use of alternative dopants, like Ga for pMOS devices. Imec reported record-breaking values for S/D contact resistivity (<10e9 Ohm.cm2) on Ga-implanted Si0.4Ge0.6 layers. However, the reported processing scheme requires an unwanted high thermal budget (laser anneal) and does not provide the necessary doping profile conformality on patterned wafers. No literature reports about epitaxial growth of highly Ga-doped SiGe or Ge by means of CVD. Indeed, major challenges need be overcome such as: 1) the low Ga solubility in Si which in turn leads to a risk for Ga precipitation and agglomeration and 2) the unwanted but expected carbon incorporation, as commercially available Ga process gases contain CxHy groups which may dissociate and/or incorporate during growth. Developing selective epitaxial growth schemes of S/D materials with higher active doping concentrations than currently available will enable the continuation of current transistor scaling. Within the frame of this internship, the candidate will generate fundamental understandings enabling the implementation of Ga-doped Ge and SiGe as S/D materials for FinFET and GAA devices. The main scientific goal of this project to understand the electrical and structural material properties of the grown materials. Particular attention will be given to the impact of defects (vacancies, Ga clusters...) and carbon incoporation on dopants activation. With respect to exploring Ga-doped Ge and SiGe as S/D materials, experimental studies will be dedicated to the extraction of contact resistivity values by means of Circular Transmission Line Measurements (CTLM).

Type of project: Thesis with internship project

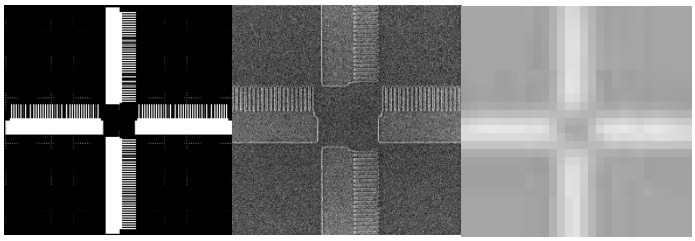
Degree: Master in Science or Master in Engineering majoring in physics, nanoscience & nanotechnology, materials engineering

Responsible scientist(s):
For further information or for application, please contact Clement Porret (Clement.Porret@imec.be) and Roger Loo (roger.loo@imec.be).

Study of an optical metrology technique for advanced semiconductor process control

Device-dimension scaling is driving the industry towards ever tighter process specifications. A key research project in the area of Advanced Patterning involves the study of an alternative metrology technique for process control at the 7 nm and 5 nm nodes. Existing in-line metrology solutions are not suited to the extensive sampling required or depend on the time-consuming validation of complex physical reconstruction models. To address the need for more efficient and cost-effective metrology, Imec recently developed and patented the Pattern Shift Response (PSR) technique: an optical solution based on asymmetric marks designed to enhance placement sensitivity to patterning variation. PSR metrology applies to lithography and throughout subsequent steps of device fabrication. To enable

deployment for semiconductor manufacturing, fundamental characteristics of PSR need to be further explored and understood.
The project entails measuring PSR asymmetric mark design variations that have been implemented on imec masks, and evaluating their efficacy using metrics such as precision, repeatability, S/N etc. to quantify their metrology capability dependence on design dimensions and some acquisition settings. On the one hand, design variations include pitch, asymmetrical pattern and reference pattern dimensions etc.; on the other hand, scaling of the acquisition zone needs to be assessed.
The marks are patterned on 300mm wafers under representative process conditions, including both DUV and EUV exposures, and measured using a high performance automated optical microscope (KLA-Tencor ARCHER 500). After training, the student will collaborate with the supervisor and the team members to design experiments, pattern wafers, create recipes, perform measurements, analyze data and develop predictive models. The overall goal is to characterize the PSR mark design space. Based on results, the student will have the opportunity to propose and implement improvements to PSR metrology and process control methods.
A good knowledge of written and spoken English is necessary for this application. The student's academic background ranges physics, optics, semiconductor technology or related engineering fields and the student shows motivation with respect to R&D in the semiconductor industry. Knowledge of automation for big data analysis will be valued in the application process (e.g. python, matlab, excel macros).



From left to right: Design, SEM picture and Optical microscope pictures of a type of asymmetrical PSR target.

More info about imec and the Advanced Patterning department:

https://www.imec-int.com/en/about-us
https://www.imec-int.com/en/advanced-patterning-and-key-process-steps

Type of project: Thesis or internship project, or combination of both

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in physics, nanoscience & nanotechnology, materials engineering

Responsible scientist(s):
For further information or for application, please contact Vincent Truffert (vincent.truffert@imec.be), Patrick Wong (Patrick.Wong@imec.be) and Kit Ausschnitt (Kit.Ausschnitt.ext@imec.be).

Spin wave-like excitations in low-dimensional ferromagnets

Integrated Circuits (ICs) are present in all electronic devices around us. In an effort to make these devices faster and cheaper, the smallest IC building blocks need to be scaled down. This further downscaling of transistors based on CMOS technology results however in a higher heat dissipation. An alternative for today's transistors is the spin wave majority gate, which is expected to have a low power dissipation when miniaturized. Genuine spin waves originate from deviations of individual, single spins with respect to the perfectly ordered ground state of a ferromagnet in which all spins are aligned parallel to each other. The waves that are propagating such deviations through the lattice of the ferromagnet are called spin waves and, as such, they can be excited only at very low temperatures. However, at room temperature one may excite similar waves, corresponding to the spatial variation of the macroscopic

magnetization vector that locally deviates from the spontaneous magnetization. Although the basic quantum theory of ferromagnetism has been established already in the previous century, various fundamental problems are left unsolved or remain to be highly controversial, especially those concerning low-dimensional magnets. Rather than relying on semi-classical theories and simulation programs, this project will focus on the fundamental physics of the spin dynamics of two-dimensional ferromagnets.
More specifically, this project addresses the time-dependent evolution of the magnetization and related quantities in order to mimic the propagation of the basic excitations and/or magnetization waves through low-dimensional magnets, such as spin wave buses or other (ultra)thin magnetic layers. Aiming at a full quantum dynamical treatment of low-dimensional spin systems, this project involves extensive computational effort, both numerically and on the theory side, where the shortcomings of commonly used classical dynamics based on the LLG equations need to be superseded. The questions that can be dealt with are: How does the local magnetization evolve in time and space? How to trigger the (phase-coherent?) propagation of elementary excitations (spin waves or spin wave-like deviations)? To which extent can we superimpose the propagation of magnetization waves, knowing that spin waves are no bosons and can therefore not be simply superimposed to generate all possible eigenstates? How detrimental is the effect of decoherence (spin-phonon interactions, spin-spin scattering...)?
Simulating the spin wave behavior in a spin wave majority gate is a very challenging task, due to its complex shape, multitude of interactions between different materials and the magnetic finite temperature excitations. Nevertheless, studying the ferromagnet at zero temperature using a simple geometry can provide already many of the desired insights. More specifically, the ferromagnet can be described as a saturated spin lattice with a Heisenberg spin Hamiltonian. Displacing some spins from their equilibrium orientation initiates a spin wave, whose dynamics is described using the Heisenberg equation of motion. The geometry itself can range from a finite spin chain up to an infinite two-dimensional lattice.
This project will involve both analytical and numerical calculations in the domains of quantum mechanics and magnetism.

Type of project: Thesis project

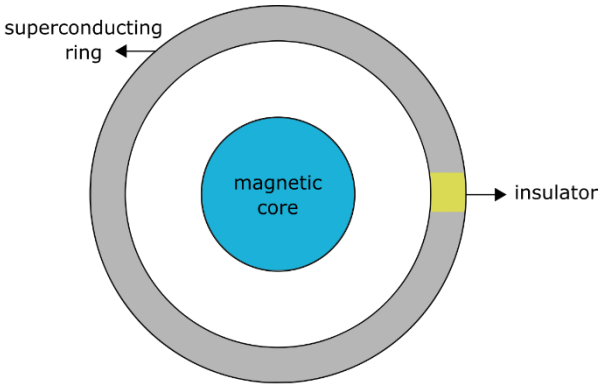
Degree: Master in Science or Master in Engineering majoring in physics, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Bart Sorée (bart.soree@imec.be), Wim Magnus (wim.magnus@imec.be) and Joren Vanherck (joren.vanherck@imec.be).

Time-dependent Ginzburg-Landau simulations for superconducting rings

Quantum computing is a new paradigm that harnesses the full complexity of the quantum-mechanical wave function to solve a computational problem. Significant interest has been given to the field of quantum information and computation since the realization that certain algorithms, such as Shor's factoring algorithm, can in principal run exponentially faster on a quantum computer, compared to a classical computer. Analogous to their classical counterparts, the fundamental unit of a quantum computer is a quantum bit, typically referred to as a qubit. Qubits are two-level systems physically realized using spins (either nuclear or electronic), ion traps, photons, superconducting circuits, etc. At present, the major scalable platform for quantum computing employs superconducting qubits based on Josephson junctions, a superconductor interrupted by an insulating barrier.
The quantization of magnetic flux lies at the heart of prospective superconducting quantum bits. When a superconducting ring is placed in a magnetic field, the lowest energy state is achieved by inducing a current that expels the field from the bulk of the ring and ensures that the enclosed flux is an integer multiple of the flux quantum, a fundamental physical constant. Accordingly, a superconducting ring exhibits a discrete spectrum of trapped magnetic flux. Furthermore, the number of flux quanta trapped within the ring can only be changed by driving part or all of the ring into the normal state. Alternatively, by introducing a weak link in the ring, for instance a thin insulating barrier that forms a Josephson junction, the flux can tunnel in and out of the ring without destroying the superconducting state.
The goal of this project is to compare the dynamics of the flux transitions in a simple superconducting ring and in a ring interrupted by a Josephson junction, referred to as rf-SQUID. The time-dependent Ginzburg-Landau (GL)

equations will be solved numerically to model the transition of a superconducting ring between the integer flux states. The model under consideration (see figure below) is a superconducting ring (with and without the insulating barrier) pierced by a core, to which the magnetic field is confined. The research plan for this project starts by a theoretical study of superconductivity, the Josephson effect and the GL equations. Next, a numerical solution for the time-dependent GL equations is pursued for a superconducting ring and for the rf-SQUID.



Type of project: Thesis project

Degree: Master in Science majoring in physics, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Bart Sorée (bart.soree@imec.be), Wim Magnus (wim.magnus@imec.be) and Ahmed Kenawy (Ahmed.Kenawy@imec.be).

Modeling of Transmon Qubits

Quantum supremacy, a term coined in 2012, is the prospect that quantum computers could solve problems that classical ones cannot by embracing the probabilistic nature of quantum mechanics. The tipping point at which quantum computers surpass classical ones is believed to be 49 quantum bits or qubits, the fundamental constituent of a quantum computer in analogy to classical bits. For this purpose, great efforts are exerted to scale up quantum computers in a race towards the first practical quantum computer.
At present, various physical realizations of quantum bits are pursued, most importantly superconducting qubits using Josephson junctions (a superconductor interrupted by an insulating barrier). Among the various implementations of superconducting qubits, the major scalable platform is currently the transmon qubit. The transmon is a variant of the charge qubit, a Josephson junction biased by a gate voltage, that operates at the regime of significantly increased ratio of Josephson energy and charging energy. As a consequence, transmons exhibit a substantial reduction in sensitivity to charge noise, while maintaining the anharmonic energy spectrum required to isolate the two-level system (TLS) defining the qubit. The noise insensitivity of transmons corresponds to a longer coherence time, i.e., the quantum state is preserved for a longer time to perform computations and to allow for error-correction.
The purpose of this project is to further improve the coherence time of transmons, a requirement for attaining highly-scalable quantum computers. The project primarily focuses on modeling transmons and the various noise sources responsible for dephasing and decoherence of the quantum state of the qubit (which can be viewed as a loss of information to the environment). Additionally, the research plan can be extended to account for the inter-qubit coupling (or, in other words, how transmons couple to each other) and how to enhance the coherence of the composite state of the overall system.

Type of project: Thesis project

Degree: Master in Science majoring in physics, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Bart Sorée (bart.soree@imec.be), Wim Magnus (wim.magnus@imec.be) and Ahmed Kenawy (Ahmed.Kenawy@imec.be).

Cross-layer memory organisation simulation and exploration framework

At imec, we are developing a cross-layer simulator framework (entitled SEAT: System benchmarking for Enablement of Advanced Technologies) intended to exploring a wide variety of memory organisations/architectures and application domain targets with different characteristics. Until now, we have mainly worked on the cache hierarchy and main memory organisation. This endeavour was carried out in close cooperation with university groups, including LIRMM at Montpellier, France. With an eye towards the future, we would like to explore the extension of the memory organisation beyond the main memory. This will be particularly useful in evaluating the impact of emerging non-volatile memories like OxRAM, CBRAM, PCM at the storage class memory (SCM) level. For this purpose, the current simulator framework has to be further extended and validated with relevant academic/commercial benchmarks. The MSc thesis focus will be on this extension, and it will especially involve working on the software framework, system architecture and incorporation of the different non-volatile memory models. The activity will happen partly at imec, Leuven and partly at LIRMM, Montpellier, in close cooperation with the team of Prof. Lionel Torres and Prof. David Novo. So it will involve a stay outside Belgium.

Type of project: Thesis project

Duration: 6-9 months

Degree: Master in Engineering majoring in computer science, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Manu Komalan (perumkun@imec.be) and Francky Catthoor (catthoor@imec.be).

Chemical mechanical polishing of new materials

Chemical mechanical polishing (CMP) has become a key step in microelectronic device fabrication: In the deposition step before CMP, an overburden of material is deposited to fill structures with metal material. During CMP, this overburden is removed, removing all metal from the field area while leaving the material inside the trenches untouched (no metal loss). In order to produce faster and more powerful commercial microprocessors, 'new' challenging materials such as copper, ruthenium, cobalt, manganese and their alloys need to be polished. For Cu-barrier CMP for example, copper etching should be limited and galvanic corrosion between the copper and barrier materials needs to be minimized. In order to design a CMP process that can achieve this, the chemical reactions that occur between the materials and the CMP slurry need to be understood and controlled. The scope of this study is to develop a CMP process for the polishing of new materials and to gain a better understanding of the mechanisms that govern this CMP process. The polishing environment is mainly controlled by two factors: the specific materials to be polished and the CMP slurry. The type and combination of materials, the thickness as well as the deposition (e.g. chemical vapor deposition (CVD), physical vapor deposition (PVD), electroless deposition (ELD) or electroplating) and annealing method can be crucial in determining CMP performance. A (metal) CMP slurry uses oxidizers, complexating agents, inhibitors and pH adjusters to achieve a fine balance of chemical reactions that remove material at the surface while keeping corrosion under control by passivating the newly exposed surface during polishing. In this project the effect of various slurry components will be studied both during polishing on our experimental polisher and in a static slurry solution in a lab environment. Surface analysis techniques like X-ray spectroscopy (XPS), X-ray diffraction (XRD) and nano-indentation will provide the necessary extra information to

understand which reactions and species are dominant at the surface. The analysis of the data will provide the understanding needed to design a model slurry which polishes the material away at a decent rate while achieving a good quality surface. If the model slurry design experiments are successful, the efficiency of the optimized slurry will be tested on blanket and/or patterned wafers to make sure that the CMP process removes the required materials with no defectivity or dishing/erosion issues. For this analysis techniques like high resolution profilometry (HRP), defectivity analysis, resistivity and ellipsometry, scanning electron microscopy (SEM) and atomic force microscopy (AFM) can be used.

Type of project: Thesis or internship project, or combination of both

Duration: 3 months

Degree: Master majoring in chemistry/chemical engineering, materials engineering, nanoscience & nanotechnology

Responsible scientist(s):
For further information or for application, please contact Lieve Teugels (teugels@imec.be).

Photoresist line edge roughness and smoothing techniques in EUV lithography

Photolithography, the process used to fabricate integrated circuits, is the key enabler and driver for the semiconductor industry for device scaling. The miniaturization of feature sizes has been achieved mainly by shortening the wavelength of exposure tools by evolutionary advances in nanolithography and in turn by similar advances in photoresist technology. Today the shortening wavelength trend is continuing with the aim of achieving 1x nm resolution by the deployment of the extreme ultraviolet lithography (EUVL) using exposure light wavelength of 13.5 nm.
Current EUV photoresist platforms have performance limitations in resolution, line edge roughness (LER) and sensitivity (RLS). LER is currently of particular interest, as nearly all resists are currently not able to meet the LER target, especially if they have to meet resolution and sensitivity target simultaneously. Furthermore, it seems that the LER does not continue to shrink down with the resolution scaling, so post processing resist treatments are needed to smooth the resist.
In this frame, the student will produce own patterned resist samples on a full field EUV scanner, he will characterize the resist roughness with the use of scanning electron microscope (CDSEM) and dedicated software for the power density spectrum (PSD) analysis. He will understand the limits from a material chemistry standpoint and will test and benchmark post processing approaches (rinse, light curing, thermal annealing, solvent annealing) of multiple patterned resists with the EUV light aiming to finally assess all the techniques taken under examination. The student will work in the international research facility of imec interacting with multiple equipment and material partners.
To accomplish his task, the student has to have, besides a chemistry or nano-technology or materials science background, basic knowledge on statistics and have liking for the design of experiments, their execution (on equipment in labs or in cleanroom) and data analysis.

$$\sigma_{LER} = \sqrt{\frac{\sum_{i=1}^{N}(x_i - \bar{x})}{N}}$$

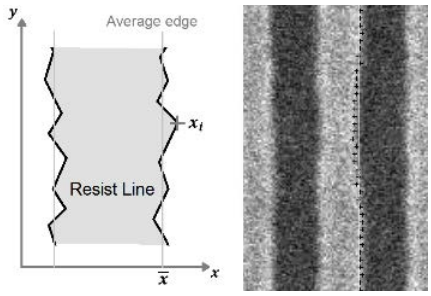


Figure 1

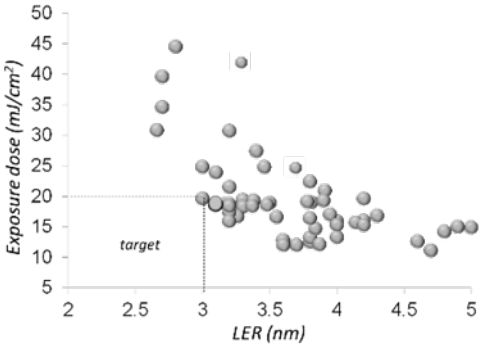


Figure 2

Figure1: LER is a measure of the variability of the pattern. Mathematically, LER for a line and space pattern, is defined as the standard deviation from the average edge for every measurement point.

Figure 2: The experimental relationship between exposure dose and LER is reported for the case of 22nm dense line-space patterning. As the exposure dose decreases the LER values get worse and it is challenging to find resists that have sensitivity and roughness both in target.

Type of project: Thesis or internship project

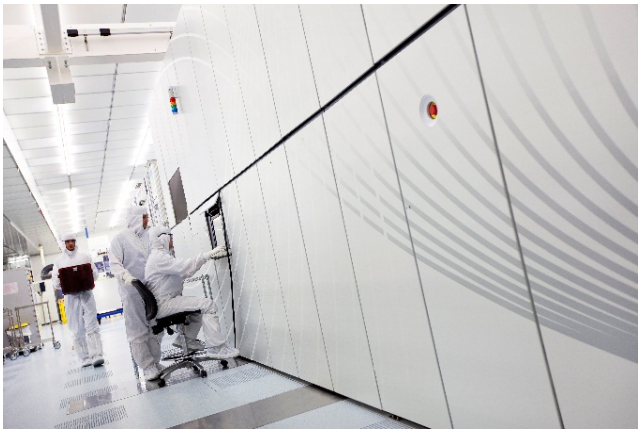
Duration: 9 months

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in chemistry/chemical engineering, materials engineering, nanoscience & nanotechnology, physics

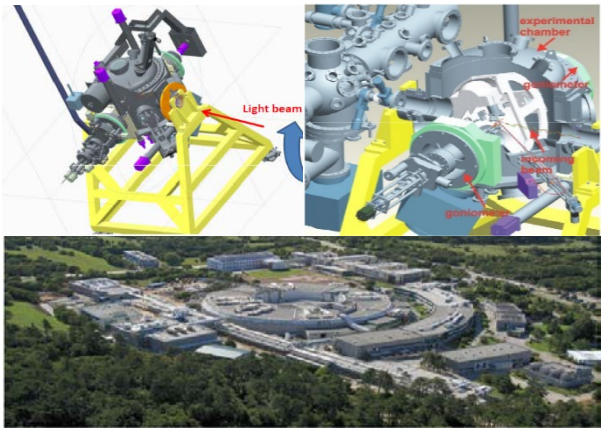
Responsible scientist(s):
For further information or for application, please contact Danilo de Simone (danilo.desimone@imec.be), Geert Vandenberghe (Geert.Vandenberghe@imec.be) and Stefan de Gendt (Stefan.DeGendt@imec.be).

Light-matter interaction in organic and inorganic photoresists for EUV lithography

Extreme ultraviolet lithography (EUVL) is the candidate to scaling down of semiconductor devices beyond the 1x nm technology node.
To realize the required EUVL targets the photoresist play a significant role and more intimate light-matter interaction studies (i.e. absorption, photo emission yield, electron efficiency, electron energy distribution of secondary electrons,..) are needed to get more fundamental understanding in their mechanism of interaction at 91.6eV (13.5nm wavelength).
In this frame, the student will work interacting with two different international research facilities.
At imec, in collaboration with material suppliers, for the design of the experiments (material selection and sample preparation), resist exposure on EUV full field scanner and data analysis.
At IOM-CNR Institute (Trieste, Italy) in collaboration with the group that is leading the CNR synchrotron beamline BEAR (http://www.elettra.trieste.it/elettra-beamlines/bear.html) at Elettra (Trieste, Italy) for the EUV-soft X-ray materials investigation and characterization including in particular photo absorption (XAS) and photoemission (UPS/XPS) spectroscopies.
This work will significantly contribute to the understanding of how different materials interact with the light and will lead to help the design of new photoresists for EUV lithography.
To accomplish his task, the student has to have fundamental understandings of x-ray, soft x-ray physics and radiation chemistry.



imec 300mm cleanroom and ASML NXE:3300 EUV tool



BEAR beamline at Elettra synchrotron facility

Type of project: Internship project

Duration: 9 months

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in chemistry/chemical engineering, materials engineering, nanoscience & nanotechnology, physics

Responsible scientist(s):
For further information or for application, please contact Danilo de Simone (danilo.desimone@imec.be), Geert Vandenberghe (Geert.Vandenberghe@imec.be) and Stefan de Gendt (Stefan.DeGendt@imec.be).

Simulations for semiconductor quantum dots

Progress in nanoscale fabrication techniques has allowed ever-smaller structures with increasing control. One fascinating result is the fabrication of quantum dots, structures where confinement is so strong that the system (at cryogenic temperatures) behaves as an artificial atom. Electrons can be loaded on to these dots one-by-one making them perfectly suited for the investigation of quantum effects. As such they're getting increasing attention in recent years due to their promising use as scalable unit blocks ('qubits') for future quantum computers.
This topic would focus on the simulation of quantum dots formed in semiconductor materials and voltage potentials applied by local gates. The student will investigate and simulate the most appropriate physical model to capture the interactions between the few electrons in the quantum dot and its environment. Different gate configurations are to be compared. Imec has a dedicated group for semiconductor simulations and the inhouse expertise would be available as an aid to the student.
We are looking for a motivated student with an interest in solid state physics and who's not afraid of some computer coding.

Type of project: Thesis project

Degree: Master in Science majoring in nanoscience & nanotechnology, physics

Responsible scientist(s):
For further information or for application, please contact Bart Soree (Bart.Soree@imec.be), Nard Dumoulin (Nard.Dumoulin@imec.be) and Ahmed Kenawy (Ahmed.Kenawy@imec.be).

Novel spin-on method to deposit self-assembled monolayers and thin polymeric films for surface and interface engineering in nano-IC applications

As the total transistors and interconnects sizes come down to few tens of nanometers and below, a shift in paradigm for the manufacture and integration of microelectronics components becomes apparent. Organic molecules - owing to their size, mechanical flexibility and chemical tunability - fit well in this slot and, thus, are expected to play a key role in IC downscaling. In this respect, self-assembled monolayers (SAMs) seem the best candidates. SAMs are a prototypical form of nanotechnology: the SAM precursor molecules carry the "instructions" required to generate an ordered, nanostructured material without external intervention. SAMs demonstrate that molecular-scale design, synthesis, and organization can generate macroscopic materials properties and functions. Although the details of the thermodynamics, kinetics, and mechanisms of assembly will differ significantly, these monomolecular films establish a model for developing general strategies to fabricate nanostructured materials from individual nanometer-scale components. Because SAMs can assemble onto surfaces of any geometry or size, they provide a general and highly flexible method to tailor the interfaces between nanometer-scale structures and their environment with molecular (i.e., subnanometer scale) precision. SAMs and polymeric films can control the wettability and electrostatic nature of the interfaces of individual nanostructures and thus their ability to organize into large assemblies and interact with overlayers adding chemical functionality, thermodynamic stability. While deposition on SAMs by dipping is already being extensively studied, SAM spin-on from organic solvents is relatively unexplored. The first phase of this project will focus on the deposition and characterization (water contact angle, FTIR, XPS, AFM, ..) of SAMs and eventually functionalized polymeric films on metal surfaces by spin-on from organic solvents. The study includes metal surface preparation before SAM deposition and the impact of post-SAM treatments such as anneal, gas flow and/or wet chemistries. The final aim of this work is to achieve a dense, ordered and defect-free SAM. In the second phase of the project we will focus on the scale-up of the SAM deposition process to 300mm wafers and on 300mm scale metrology techniques, such as light scattering, AFM, ellypsometry, mass measurement.

Type of project: Internship or thesis project, or combination of both

Duration: 6-12 months

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in chemistry/chemical engineering, materials engineering

Responsible scientist(s):
For further information or for application, please contact Silvia Armini (armini@imec.be).

Fundamental study of SiCO, poly Si and SiO2 in Quasi-atomic layer etch mode

Progressively downscaling of CMOS Logic devices towards 7 nm node and beyond, requires highly accurate patterning processes (dry etch). The process flow is complex and the patterning steps require utmost precision because of the complex stacks of thin layers. Dry etch contrast is a key requirement for these thin layers: SiCO, Poly Si and SiO2. In this work, the student will focus on the in-depth understanding of the quasi atomic layer etch (Q-ALE) mechanism. In these dry etch processes, short gas injection cycles (radical fluxes) alternate with accurately controlled ion fluxes to target angstrom precision feature patterning. In this work, the student will focus on the in depth understanding of the etch mechanism. There will be a link with the area selective deposition research as controlled selective polymer deposition is a common goal in both fields.
The goal of the study should be bi-lateral:

1. The student will get an in-house training on etch tool operation and working in a 300 mm clean room according to the safety rules. He/she will get familiar with measurement tools like: thickness measurement (ellipsometry), mass measurements, TOFSIMS, XRR. Next to that, he/she will get a basic training/understanding of plasma etch as he/she will operate the etch tool fully independently. Our etch literature library will be available to help him/her understanding the etch processes and key parameters that control the process.

2. The student should gain insight in the etch mechanism and process window control of Q-ALE at the end of the internship. The idea is to study the plasma parameter space (pulsing, TCP power, bias power, gas nature, chuck temperature, Ar flow, ...) that affects the nature of the deposited CFx polymer and the etching of the blanket substrates. The best performing process conditions can be morphologically verified on relevant topography wafers. The practical work can be completed with a literature study on the specific etch plasma's. At the end of the internship all the results should be compiled in a scientific report.

Type of project: Thesis with internship project

Duration: 6 months

Degree: Master in Engineering Technology or Master in Science majoring in chemistry/chemical engineering, materials engineering, nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information or for application, please contact Efrain Altamirano Sanchez (Efrain.AltamiranoSanchez@imec.be) and Geert Mannaert (Geert.Mannaert@imec.be).

Modeling of magnetoelectric coupling for advanced spintronic applications

Spintronics is a novel field of electronics that uses the spin of electrons or the magnetization of thin films instead of charge in memory or logic computation devices. A key issue of spintronics is the energy-efficient control of the magnetization in such devices. Current device concepts are often based on the control of the magnetization by currents, for example via generated magnetic fields or recently discovered effects, such as spin-transfer torque or spin-orbit torque. However, such techniques are typically not very energy-efficient and it would be very desirable to control the magnetization by electric fields instead. In principle, this can be done by the magnetoelectric effect, which couples electric fields to the magnetization. This effect is currently strongly considered to be included in future generations of low-power spintronic devices.
Magnetoelectric effects naturally occur in multiferroic materials but much stronger strain-induced magnetoelectric coupling can be observed in composite materials consisting of piezoelectric and magnetostrictive materials. The application in spintronic devices requires a detailed understanding of the effects of the geometry (e.g. the relative directions of the electric field and the magnetization) as well as thermal fluctuations on the magnetization dynamics. In this thesis, the student will perform micromagnetic simulations to study the magnetoelectric coupling in different geometries and different material systems. An important parameter will be the magnetocrystalline anisotropy of the magnet. The goal of the thesis is to develop efficient strategies to excite, control, and detect magnetization dynamics (including both magnetic switching as well as spin waves) by the magnetoelectric effect and transfer them to a magnetic waveguide. The work will be in close collaboration with experimentalists working on integration of magnetoelectrics into spintronic devices for beyond CMOS logic.

Type of project: Thesis project

Degree: Master in Science majoring in nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information or for application, please contact Christoph Adelmann (christoph.adelmann@imec.be), Florin Ciubotaru (florin.ciubotaru@imec.be) and Adrien Vaysset (adrien.vaysset@imec.be).

Spintronic devices based on spin waves for beyond CMOS applications

Spintronic devices based on spin waves are promising alternatives to the CMOS technology and have high potential for power and area reduction per computing throughput. The information can be encoded in either the amplitude or the phase of the wave, while the logic operation is based on the interference of spin waves, which is a keystone for the realization of logic gates. To be competitive with actual CMOS technology the spin wave devices need to tackle waves with wavelengths below 100 nm and a miniaturization down to the nanoscale. Thus, the understanding of the properties of spin waves as their generation and propagation, the phase control and the interference mechanism at the nano-scale are of fundamental importance for the realization of the logic gates.
Within this thesis project, the student will fabricate spin-wave devices based on different magnetic materials, from micro- down to the nanoscale and will contribute to their characterization in the microwave frequency range leading to important properties as spin wave dispersion relation, their damping and their propagation characteristics in the linear and non-linear regimes, including a phase analysis. The results will be an important step to understand the emission, the routing and the combination/interference of spin waves to continue the assessment of the concept devices as alternatives or complements to CMOS transistors in future technology nodes. The experimental work will be performed in close collaboration with modeling activities (materials, devices, circuits) in the spintronics group at imec. The student should have a strong interest in nanofabrication in a cleanroom environment as well as in leading edge research topics on magnetism and magnetic materials.

Type of project: Thesis or internship project, or combination of both

Duration: 6 months

Degree: Master in Science or Master in Engineering majoring in nanoscience/nanotechnology, physics, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Christoph Adelmann (christoph.adelmann@imec.be), Florin Ciubotaru (florin.ciubotaru@imec.be) and Iuliana Radu (Iuliana.Radu@imec.be).

Reliability assessment of RRAM memory devices

Memory devices based on resistive switching, the so-called Resistive Random Access Memory (RRAM), are currently considered as strong candidates for next-generation memory applications. The switching mechanism relies on the voltage-driven electrochemical formation/dissolution of a conductive filament in a solid electrolyte, leading to the commutation between a high-resistive state (HRS) and a low-resistive state (LRS) and vice versa. A typical RRAM device consists of an electrically insulator film, where the resistive switching occurs, sandwiched between two electrodes[1]. Promising features, such as scalability potential [2], fast and low-current operation, long-endurance lifetime, and good data retention[3-4], have already been reported for RRAM devices. However, the reduction of the operating power, which is crucial for aiming at Internet of Things (IoT) applications, induces a large increase in the state variability and a deterioration of the memory performances, hindering a massive introduction of this technology in the memory market. This internship will focus on the electrical characterization and reliability assessment of cutting-edge RRAM devices for low-power applications, to outline the impact of materials and integration schemes on the memory performance and to identify the root causes of reliability failures for proposing further improvement of the stacks. You will be trained in the use of advanced electrical characterization tools and you will carry out reliability assessment by using state-of-the-art characterization techniques, benchmarking different RRAM technologies. Careful and critical data analysis will be an essential part of the task, as well as proposing alternative characterization strategies for effective reliability assessment. You will work in a dynamic R&D environment and you will be expected to regularly present and discuss your results with a team of experts in the field. Therefore, a proficient use of English is also required. A good command of data analysis softwares (Matlab, Origin, etc.) will be considered a strong plus.

[1] R. Waser et al., "Redox-Based Resistive Switching Memories – Nanoionic Mechanisms, Prospects, and Challenges", Advanced Materials, 21, 2632-2663 (2009)
[2] B. Govoreanu et al., "10×10nm2 Hf/HfOx crossbar resistive RAM with excellent performance, reliability and low-energy operation", IEDM Tech. Digest, 729-732 (2011)
[2] S. Sills et al., "Challenges for High-Density 16Gb ReRAM with 27nm Technology", VLSI Tech. Digest, T106 (2015)
[3] A. Belmonte et al., "A Thermally Stable and High-Performance 90-nm Al2O3\Cu-Based 1T1R CBRAM Cell", Trans. On El. Devices, 60 (11), 3690-3695 (2013)

Type of project: Thesis or internship project, or combination of both

Duration: minimum 3 months

Degree: Master in Science or Master in Engineering majoring in nanoscience/nanotechnology, physics, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Attilio Belmonte (attilio.belmonte@imec.be) and Andrea Fantini (andrea.fantini@imec.be).

Magnetism in graphene for spin-orbit torque (SOT) devices

Magnetic random access memories (MRAM) are foreseen to be the most credible non-volatile memories, which are low power, high endurance and fast enough to compete with cache CMOS elements. So far, spin transfer torque (STT) is the mature mechanism used to write magnetic tunnel junction (MTJ) which are at the core of MRAM bit cells, however, there is a need for exploring new concepts and new material systems to overcome STT-MRAM limitations. Meanwhile, strong effort has been devoted on creating and manipulating magnetism in two-dimensional graphene layer and its further implementation in spintronic-based MRAM devices. Graphene has already shown the possibility to propagate spins over a very long distances [1,2]. However, pristine graphene only exhibit Landau orbital diamagnetism, not yet suitable to use it as the magnetic bit for the memory element. There may be the possibility that the long range ferromagnetic ordering can be introduced in bybrid graphene non-ferromagnetic metals (diamagnetic Cu and paramagnetic Mn) by the mechanism based on magnetic hardening of the metal atoms [3]. Nevertheless, graphene allows to manipulate the magnetic anisotropy energy in existing ferromagnetic materials (Co) via the hybridization between the π-orbitals in graphene and the nearby spin-polarized d-orbitals in magnetic materials [4] that can help to reduce the material stack in the currently used MRAM. All these advanced and innovative concepts open up the path to novel graphene-based spintronic devices and the possibility to create and manipulate spin current through spin-orbit effects for future non-volatile MRAM application.
Imec has demonstrated in the past years the capacity to produce state of the art STT-MRAM. Furthermore, imec is currently developing methods for large scale growth and transfer of high quality 2D materials (graphene and others). Therefore, imec offers a unique possibility to bridge these two worlds for magnetic-memory related activities, in a FAB environment. Below are the main task to be performed during this internship part of the Exploratory magnetic memory project of imec. It will be mostly consist of graphene transfer (20%), nano-fabrication (40%), magnetic and electrical characterization (30%), and literature (10%).

I. Different transfer methods of chemical vapour deposition grown graphene on SiO2 or on other given substrates.
II. Fabrication of hybrid graphene-metal heterostructure Hall-bars and magnetic tunnel junctions (MTJs).
III. Characterization of the magnetic properties and spin-orbit effect by measuring Hall effect and tunnel magnetoresistance (TMR).

[1] N. Tombros et al., Nature (2007), [2] S. Roche et al., 2D Materials (2015); [3] F. A. Ma'Mari et al., Nature (2015); [4] H. Yang et al., Nano Lett. (2016).

Type of project: Thesis project or thesis with internship project

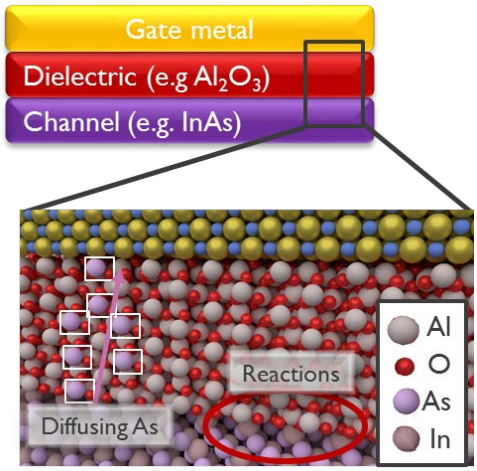
Duration: 6 months

Degree: Master in Engineering majoring in nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information or for application, please contact Kevin Garello (Kevin.garello@imec.be) and Subir Parui (Subir.Parui@imec.be).

Thermal degradation mechanisms in III/V – dielectric stacks & potential improvements in material quality for future CMOS applications

Computers, cellphones, etc. have seen a continues increase in performance and potential ever since they were invented centuries ago. We all take this as a given, and for many years it was, to increase performance the task was to shrink down the elementary building blocks so more could fit onto a given area. But this trend is coming to a halt as it is getting harder and harder to go smaller. So now, new strategies are needed to allow the performance of these appliances to keep increasing are needed. One of these strategies consist of introducing new materials and treatments and has already shown great potential.
In this project, you will work on a promising class of semiconductors know as III-V alloys. These materials promise a remarkable increase in performance and reduction in power which would make them candidates for everything from supercomputers to making your cellphone consume less. Of course no innovation comes without its challenges, for III-V this challenge lies in a lower thermal stability than the current material of choice (Si).
Consider the two elementary components found in transistors, namely the (III-V) channel (through which the current flows) and the dielectric (which allows isolates gate and channel and allows the buildup of an electric field) . This dielectric generally has a lot of structural defects that need to be cured by applying temperature. However, combining that with a thermally unstable channel is no easy task. The goal of this project is thus to come to a deeper understanding of the mechanisms at play in this III-V/dielectric stack as temperature increases. What trend does the curing of the dielectric follow with temperature? At what point will the III-V material start to destabilize and diffuse through the dielectric, at what rate? Could we potentially find a dielectric that acts as a diffusion barrier thus allowing higher temperatures to be achieved?



These are all interesting questions, answering of which will bring help realize faster and more reliable devices for the future.
As part of the project the student will investigate the mechanisms at play at different temperatures (diffusion, reactions, intermixing, ...). To do this samples of III-V materials capped with several dielectrics are available which can be given a thermal budget (temperature ,time, atmosphere(N2 vs H2,...) and analyzed using the many chemical/physical characterization techniques available on the IMEC site. The starting point of this project will be the knowledge base already gathered on thermal stability of these materials in the research group.
All trainings (techniques, tools,...) will be provided as part of the thesis.

Type of project: Thesis project

Degree: Master majoring in chemistry/chemical engineering, materials engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Dieter Claes (Dieter.Claes@imec.be).

Defect reduction in directed self-assembly processes

With scaling of electronic devices, printing smaller structures on the chip has become more and more complex and costly. For a few years, directed self-assembly (DSA) has been considered as a viable and low-cost alternative and complementary patterning option for keeping the down-scaling alive in the coming years, while ensuring an economic benefit to the silicon industry. Instead of upgrading lithography tools and imaging materials, DSA process uses block copolymers that can spontaneously form 5 - 30 nm features to print fine pattern. Several figures of merit have been identified and put forward as major checkpoints to assess the relevance of DSA processes for high-volume manufacturing environment; defectivity, roughness, placement accuracy, repeatability, and cost of development. Your project will focus on one of the main factors that would make or break the show for DSA to be adopted by the IC manufacturers/production fabs – reducing the number of defects on the wafer after DSA and to be able to identify their root causes. The main goal of your Masters' thesis/internship is to support and enable the defect reduction strategies of the DSA program at imec. From this project, you will first get accustomed to advanced lithography tools in our 300 mm wafer production line environment. As you get familiar with the DSA process and defect inspection techniques, the focus of your study will shift more towards automated defect review/classification capabilities using a 300 mm in-line review SEM and a dedicated software. A big part of your tasks will also include running the weekly defectivity monitor flow and analyzing the data from it, which acts as the baseline to assess the impact of the various defect reduction approaches we adopt. [Generic DSA literature] 1) H.S. Philip-Wong et al., Block Copolymer Directed Self-Assembly Enables Sublithographic Patterning for Device Fabrication, Proc. of SPIE Vol. 8323, 832303, 2012. doi: 10.1117/12.9183122. 2) W. Hinsberg et al., Self-Assembling Materials for Lithographic Patterning: Overview, Status and Moving Forward, Proc. of SPIE Vol. 7637 76370G, 2010. doi: 10.1117/12.852230 [Project specific literature] 1) P. Delgadillo et al., Defect source analysis of directed self-assembly process (DSA of DSA), Proc. of SPIE Vol. 8680, 86800L, 2013. doi: 10.1117/12.2011674 2) P. Delgadillo et al., All track directed self-assembly of block copolymers: process flow and origin of defects, Proc. of SPIE Vol. 8323, 83230D, 2012. doi: 10.1117/12.916410 3) C. Bencher et al., Directed Self-Assembly Defectivity Assessment, Proc. of SPIE Vol. 8323, 83230N, 2012. doi: 10.1117/12.917993 27

Type of project: Internship or thesis project

Duration: 12 months

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in chemistry/chemical engineering, materials engineering, nanoscience/nanotechnology, eletrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Hyo Seon Suh (Hyoseon.suh@imec.be), Paulina Rincon Delgadillo (Paulina.RinconDelgadillo@imec.be) and Geert Vandenberghe (Geert.Vandenberghe@imec.be).

Transmission electron microscopy: more than an image

Transmission electron microscopy (TEM) is an indispensable analysis technique for the development of advanced 3D semiconductor devices. It allows imaging of device structures with very high spatial resolution in different modes as well as chemical analysis of the local composition with sub-nanometer resolution. Interpretation of the images for metrology purposes is generally directly possible. However more advanced interpretation for extracting detailed (quantitative) materials properties requires further analysis of the images or spectra. E.g. strain analysis at defects and in devices can be done in several ways based on either high resolution lattice images or diffraction patterns, compositional analysis can be based on image contrasts or with X-ray or energy loss spectra, etc. For all these

applications several software packages exists. The obtained results will be dependent on selected parameters and procedures in the software and may depend on the used software program.
The work is focusing on the evaluation and comparison of different software packages for advanced interpretation of TEM results and application to different topics (strain, compositional analysis) making use of the vast database of TEM measurements available at imec. The goal will be to determine best practices for several use cases and applications. It will require that the student obtains an excellent insight in the basics of electron beam/materials interactions and TEM image formation as well as of the materials properties that are investigated. Background or high interest in crystallography is therefore needed. The work is not focusing on software development or own use of the TEM instruments.
Ref : ImageEval ; http://en.wikipedia.org/wiki/Multislice ; http://tem-s3.nano.cnr.it/?page_id=2

Type of project: Internship project

Duration: 6 months

Degree: Master in Science majoring in materials engineering, physics

Responsible scientist(s):
For further information or for application, please contact Hugo Bender (hugo.bender@imec.be).

3D chemical analysis of microelectronics systems

One driver of the semiconductor industry growth is the sustained realization of "Moore's Law", whereby the number of transistors in an integrated circuit doubles approximately every 2 years with an associated increase in circuit functionality, reduction in operational power, and, most important, a reduction in unit cost. These fast technological developments, including increased process and material complexity, as well as reduced tolerance levels for process excursions have increased the need for a more controlled manufacturing environment necessitating equivalent improvements and developments in metrology. The present evolution towards merging lab and Fab metrology implies that these developments are necessary for use both in the R&D phase as in the final production phase. With the strong size dependence of many material problems and phenomena, metrology needs to be performed more and more on devices with realistic dimensions and on wafer scale. Imec has recently acquired a new metrology tool combining a TOF-SIMS (Time of Flight Secondary Ions Mass spectrometry) and an AFM (Atomic Force Microscope) instrument. This instrument is designed in order to combine chemical information from the TOF-SIMS with topographical information from the AFM, allowing 3D chemical mapping of samples. The objective of this thesis is to establish this TOF-SIMS-AFM system as a 3D-metrology tool. For this objective, the AFM module will be used purely in topographic mode. The first part of the thesis will be devoted to the qualification of this new instrument to establish its ultimate performances, before applying it to model system. These systems will be chosen from technologies from the BackEnd-Of-Line (dual damascene). In these systems, etching of trenches occurs via a Reactive Ion Etching step, leaving polymer residues on the structures. These residues need first to be cleaned before metal deposition can occur and a detailed chemical analysis is frequently needed to determine the optimum cleaning process and its efficiency. This can be evaluated by XPS on specifically designed structures . However, the information content of TOF-SIMS for organic contaminants is much higher than from photoemission, hence TOF-SIMS is a preferred analysis approach. Unfortunately, the topography on the line arrays prevents a full 3D reconstruction of TOF-SIMS profiles. The application of the 3D-TOF-SIMS system using the in-situ AFM represents an important step forward in this case. After filling the trenches with Cu, one still has no or limited physico-chemical information on the 3D Cu concentration in the ILD between Cu lines. A prominent challenge one faces in analyzing these structures, is that when using sputtering for depth profiling, topography is developing during the analysis due to large difference in erosion rate between the different materials. This thesis will show that this problem can be solved using TOF-SIMS-AFM by monitoring the topography growth and implementing correction procedures. The output will be protocols for quantitative composition profiles for heterogeneous and non-planar systems.

Type of project: Thesis with internship project

Duration: 6 months

Degree: Master in Science or Master in Engineering majoring in materials engineering, physics, chemistry/chemical engineering

Responsible scientist(s):
For further information or for application, please contact Alexis Franquet (Alexis.Franquet@imec.be), Valentina Spampinato (Valentina.Spampinato@imec.be) and Wilfried Vandervorst (Wilfried.Vandervorst@imec.be).

Compositional inaccuracies in laser-assisted atom probe tomography: the case of B-doped SiGe

Targeting enhanced transistor performance at every technology node has taken the semiconductor industry very far from the good old planar Si transistor described in most textbooks. First of all, material wise, state-of-the-art transistors not only contain Si but also a variety of different materials such as SiGe(Sn), high-K and potentially III-V materials in a near future. On top of it, transistor architectures have also evolved toward three-dimensional structures embodied by the latest 7-nm fin field-effect transistors (finFETs).
As semiconductor devices undergo these dramatic changes, metrology has to adapt. Consequently, there is a growing need for metrology techniques that can provide three-dimensional information at the sub-nm scale about parameters critical to device performance such as composition and dopant distribution. In this context, Atom probe tomography (APT) has emerged as one of the most promising technique to solve these many needs. APT is a powerful metrology technique that can indeed offer 3D information with near-atomic spatial resolution (~0.2-0.3 nm) and high chemical sensitivity (10 ppm). This technique is based on controlled field-evaporation of atoms from a needle shaped specimen (apex ~100 nm). Voltage or laser pulses are used to trigger the field evaporation of atoms which are then collected on a position sensitive detector. However, the technique suffers from serious compositional inaccuracies due to the elemental dependence of the field evaporation mechanism the technique is based upon. The latter dependence leads to a preferential retention of some species on the specimen, i.e. inaccurate composition is measured. In turn, as has also been observed, the retained atoms tend to move along the specimen surface before being evaporated, i.e. major artefacts in their lateral distributions are also measured.
In this project, we propose to look experimentally and theoretically at the quantification of B-doped SiGe in laser-assisted APT. The selected candidate will run atomprobe measurements on dedicated tips of known geometries. The known tip geometry will help the quantification as the number of atoms of each species can be evaluated from the measured volume. Simulations will also be used to evaluate the efficiency of retention and migration when changing the measurement conditions, i.e. voltage and laser power.
This work will be done in the characterization group of imec offering multitude of characterization techniques in support of this project. It will also be done in very close collaboration with the process engineers of imec and its industrial partners.

Type of project: Thesis or internship project, or combination of both

Duration: 6 months

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in materials engineering, physics, electrotechnics/electrical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Claudia Fleischmann (Claudia.Fleischmann@imec.be), Janusz Bogdanowicz (Janusz.Bogdanowicz@imec.be) and Wilfried Vandervorst (Wilfried.Vandervorst@imec.be).

Fabrication and evaluation of diamond tips and probes for 3D nanoscale measurements

Diamond is outperforming other materials in many domains such as hardness, wear resistance, thermal conductivity, chemical inertness, and biocompatibility. As it can be made electrically conductive (p-type) by boron doping, boron-doped diamond thin films look especially attractive for electrical applications. At imec, we have developed electrical probe tips made from boron-doped diamond which allow for the nanoscale electrical measurements of most advanced transistor structures using scanning probe microscopy (SPM). There is currently an increasing trend to perform such nanoscale measurements also in a three-dimensional (3D) way using a so-called slice-and-view approach whereby iterating between nanometer-thick materials removal scans and measurement scans. As the existing diamond tip technology is designed for two-dimensional (2D) methods, it needs to be adapted and improved for supporting such 3D measurement concepts in an optimal manner.
The goal of this internship is to support the development of advanced diamond tips targeting 3D slice-and-view based SPM measurements. For this, the student will design the required lithography masks, perform diamond growth by chemical vapor deposition (CVD), carry out the fabrication steps for tips and probes, and assess the performance of the fabricated probes by SPM.
For this topic, the student will work inside a cleanroom and lab environment to carry out the required experimental steps. The student will characterize the fabricated tip sensors using SPM. The student will be part of imec's materials and component and analysis group.

Type of project: Thesis or internship project, or combination of both

Duration: 6 months

Degree: Master in Science or Master in Engineering majoring in materials engineering, physics, electrotechnics/electrical engineering, nanoscience/nanotechnology, chemistry/chemical engineering, mechanical engineering

Responsible scientist(s):
For further information or for application, please contact Thomas Hantschel (Thomas.Hantschel@imec.be).

Detector arrays bringing novel capabilities to Rutherford backscattering spectrometry

At imec a wide variety of front edge nano-electronic devices and applications (transistors, memories, solar cells,...) are being investigated and developed. For this, more powerful characterization techniques are necessary to assist in the development of the extremely challenging new devices (9 nm technology). High-energy ion beam based materials characterization (a.o. known as Rutherford backscattering spectrometry - RBS) is a powerful approach to study nanostructures. For this, imec operates a 2 million Volt ion accelerator connected to high-vacuum detection end-stations and unique data-acquisition electronics. The experimental results are then compared to physical models to quantify and understand the properties of the novel devices.
To date, RBS is mainly used on thin films to measure the composition and thickness. The project aims to employ the newest data-acquisition infrastructure and multi-detector systems (available at imec) to develop High-Sensitivity RBS and RBS-tomography, i.e. novel characterization methods for ultra-ultra-thin depositions in area-selective ALD growth, for nanowires, and even for 3D nanostructures.
Using advanced technology originally developed for high-energy physics and recently first applied to ion beam materials characterization at imec, we are able to configure a multi-detector configuration strategically tailored to a specific problem.
For a selected problem statement, you will be involved in the geometric design of the detector configuration. You will optimize the detector configuration based on fundamental understanding and simulations. You will participate in the practical implementation of the detector system and in the execution of the experiments at the accelerator.

Using state-of-the art analysis software (collaboration with M. Mayer from Max-Planck-Institut für Plasmaphysik, Garching) you will analyze the acquired spectra to extract properties of the nanostructures, and even propose further improvements to the experimental approach as well as to the modelling.
This project will give you in-depth experience in state-of-the art materials characterization, using a high-energy accelerator and applied to area-selective ALD and confined 2D and 3D nanostructures. You will familiarize yourself with technologies that are key in future nano-electronics nodes. The project is especially interesting if you further on wish specialize (e.g. through a PhD) in materials characterization, materials engineering, as well as in device integration engineering.

Type of project: Thesis project, or combination of thesis with internship

Duration: 6 months

Degree: Master in Science or Master in Engineering majoring in materials engineering, physics, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Johan Meersschaut (Johan.Meersschaut@imec.be).

Adaptive control of an accelerator based measurement system

A wide variety of front edge nano-electronic devices and applications (transistors, memories, solar cells,...) are investigated at imec. To verify the properties of the extremely challenging new devices (sub-22 nm technology) high-end characterization tools are essential. In this framework accelerator based characterization is one of the approaches that is pursued. For this, imec operates a 2 million Volt tandem particle accelerator, connected to multiple beam-lines and high-vacuum detection end-stations. Continuous investments in hardware and detection systems allow us to be internationally at the forefront in terms of ion-beam based characterization of nano-electronic devices.
This project aims to improve and further develop the control application (WASP) originally developed at imec. The WASP project enables to control a medium-large dynamic constellation of instruments in a modular and naturally multi-threaded way. In particular, the software allows to communicate with single devices through Ethernet (TCP/IP) and RS232/RS485 (via Serial-Ethernet gateways) and with the user through a user-friendly graphical interface (GUI) as well as support for a flexible scripting language capability. The signals from various virtual instruments are accessible to both the GUI as well as to scripts that can be run in a command-like environment.
To date, the focus was to achieve a passive control of the apparatus, in other words to obtain a scripted (pre-defined) operation. The aim is now to develop adaptive control, i.e. to use readout signals from the tool to optimize the operation.
The main tasks will be:

- To implement a communication driver (so-called daemon or service) in C/C++, to read out analog values from the tool (read-parameter), and to implement a corresponding graphical user interface in HTML + Javascript to run with Windows' Hypertext Application environment (HTA).
- Similarly to implement a communication driver to digitally control an analog parameter of the tool (set-parameter).
- To design and implement adaptive control of the set-parameter based on the value of one or more read-parameters, using for example PID or fuzzy logic. It includes the design of the feed-back mechanism and the comparison of the suitability of C/C++ and Python.

The project covers aspects of human-machine interfacing, automation and smart systems.

Type of project: Thesis project, or combination of thesis with internship

Duration: 6 months

Degree: Master in Engineering Technology majoring in computer science, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Johan Meersschaut (Johan.Meersschaut@imec.be).

Development of NV-diamond tip sensor with electrical readout

The nitrogen-vacancy (NV) defect center in diamond gained recently a lot of interest as its spin state is extremely sensitive to magnetic and electric fields, pressure, and temperature and looks therefore very promising for sensing applications. In the most simplified way, the changes of NV spin resonance frequency are directly proportional to the external fields. Various NV-diamond sensors have been demonstrated for use in scanning probe microscopy (SPM) whereby the NV spin readout is realized via the principle of optical detection of magnetic resonance (ODMR). One of the disadvantages of this signal detection approach is that it is due to its large dimensions not well suited for integrating NV-based sensors and devices into future nanoelectronics chips. Therefore, the so-called photo-electrical detection of magnetic resonance (PDMR) method has been proposed and demonstrated as an alternative by UHasselt and imec. The integration of the PDMR readout into a scanning probe sensor would be an important milestone towards NV center-based sensor and device integration into nanoelectronics circuits.
The goal of this internship is to support the development of NV-diamond tip sensors with electrical readout. For this, the student will develop and fabricate NV-diamond tips, will add metal electrodes to these tips for electrical readout, and will integrate such tips into a scanning probe sensor. Hereby, the student will utilize imec's broad fabrication knowhow for electrical diamond probes.
For this topic, the student will work inside a cleanroom and lab environment to carry out the required experimental steps. The student will characterize the fabricated tip sensors using SPM. The student will be part of imec's materials and component and analysis group.

Type of project: Internship or thesis project, or combination of both

Duration: 6 months

Degree: Master in Science or Master in Engineering majoring in chemistry/chemical engineering, electrotechnics/electrical engineering, materials engineering, mechanical engineering, nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information or for application, please contact Thomas Hantschel (Thomas.Hantschel@imec.be).

Composition measurements in advanced III-V nanostructures using Raman spectroscopy

One of the next steps in future-node semiconductor technology is the use of III-V compound semiconductors as a high-mobility channel material. The growth of these alloys on industry-standard Si wafers is challenging and may lead to the introduction of defects and compositional fluctuations. Accurate measurements of the latter are particularly difficult given the high surface-to-volume ratio of the structures and the large lattice mismatches with the substrate. In this topic, the use and optimization of micro-Raman spectroscopy is investigated for measuring the local composition in next-generation semiconductor architectures. Raman spectra for III-V materials are in general quite complex and the small dimensions of the region of interest further complicate the measurement. However, it was recently found that a nano-focusing phenomenon enables the confinement of the excitation light inside the structures, leading to considerable enhancement of the Raman response. The internship will involve experimental work on state-of-the-art transistor structures combined with the development of a thorough understanding of the III-V Raman coupled modes. The resulting compositional measurements will be correlated with complementary metrology but

the experimental work focuses on the Raman spectroscopy. The student will learn to work with a micro-Raman system using different laser wavelengths. A strong physics background is required. The student will be trained in working with a Raman system and characterize advanced semiconductor device structures. He/she will be part of the materials and component analysis (MCA) department.

Type of project: Internship project

Duration: 6 months

Degree: Master in Science or Master in Engineering majoring in materials engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Thomas Nuytten (thomas.nuytten@imec.be).

Electrical SPM characterization of 2D semiconductors

In recent years, two-dimensional 2D transition metal dichalcogenides (2D TMDs) have been the focus of intense investigation as a potential replacement for Si in logic devices. Theoretically, 2D TMDs should be able to achieve high mobilities and large Ion/Ioff ratios. Nevertheless, real devices suffer from defects, nano-scale inhomogeneity, and the effects of processing that significantly limit their performance. Due to the true 2D nature of these materials, scanning probe microscopy (SPM) techniques are an ideal tool for investigating the electronic properties of 2D materials and devices.
The goal of this thesis/internship will be to identify and gain understanding into the primary impediments to high performance 2D field effect transistors (2D-FETs). This project will employ electrical SPM to characterization single atomic layer or few layer MX2 materials, typically MoS2 and WS2, equipped with a backgate, allowing for the electrostatic control of the carrier density. SPM measurements will be correlated with other characterization techniques, specifically electrical transport. The student will be trained in advanced electrical SPM techniques, starting with Conductive Atomic Force Microscopy (C-AFM) and Kelvin Probe Force Microscopy (KPFM), and will use them extensively throughout the thesis/internship. Other techniques may also be explored, as dictated by the needs of the project. Data interpretation and analysis will also be a major part of the thesis/internship. As such, the student will be guided in design of the experiment and understanding the resulting experimental data. Furthermore, the student will be integrated into a multidisciplinary R&D team and will be expected to give periodic presentations on the status of the project. A good command of English is required.

Type of project: Internship or thesis project, or combination of both

Duration: 6 months

Degree: Master in Science or Master in Engineering majoring in materials engineering, nanoscience/nanotechnology, physics, chemistry/chemical engineering, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Jonathan Ludwig (Jonathan.ludwig@imec.be) and Kristof Paredis (Paredis@imec.be).

Electrical SPM for 3D carrier quantification

Over the past few decades semiconductor technology nodes have been witnessing a continuous downscaling for their performance increase. With the recent emergence of 3D architecture i.e. FINFETs and Nanowires, it has become very important to develop a characterization technique which is able to probe quantitatively the extremely

localized active dopants within these confined devices with sub nm resolution. Electrical Scanning Probe Microscopy techniques such as Scanning Spreading Resistance Microscopy and Scanning Capacitance Microscopy are well-established for 2D carrier profiling with the ability to expand their horizon to 3D. However, the presence of interfaces and confined current paths in devices impact the final measurement severely and hence prevents the precise quantification of carriers. Therefore, in case of confined volumes, dedicated experiments are needed to be performed to study the impact of junctions and interfaces on final measurements. This project aims at understanding and mitigating the problems associated with 3D carrier profiling with nano scale SPM techniques and developing a robust quantification method. During this internship, the student will be trained on the SPM tools and will focus on understanding the electrical characterization of materials and devices. The student will be a part of the SPM team within imec's materials and component analysis group. A good command in English is expected from the student.

Type of project: Internship or thesis project

Duration: 6 months

Degree: Master in Science or Master in Engineering majoring in nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information or for application, please contact Kristof Paredis (Paredis@imec.be).

Predicting dielectric breakdown voltage in MOSFETs: the missing link?

Time-dependent gate oxide breakdown (or time-dependent dielectric breakdown, TDDB) is a failure mechanism in MOSFETs, when the gate oxide breaks down as a result of the application of an electric field. The breakdown is caused by formation of a conducting path through the gate oxide to substrate due to electron tunneling current, when MOSFETs are operated close to or beyond their specified operating voltages. Breakdown models can be used to predict the time to fail for the component due to time dependent dielectric breakdown (TDDB). The most commonly used test for the investigation of TDDB behavior is constant voltage stress, whereby a voltage is applied to the gate, while its leakage current is being monitored. The time it will take for the oxide to break under this constant applied voltage is called the time-to-failure. The test is then repeated several times to obtain a distribution of time-to-failure. These distributions are used to create reliability plots and to predict the TDDB behavior of oxide at other voltages. [1] A huge disadvantage of this type of measurements is that they can take a very long time. A test-method that can estimate the gate oxide immunity in a short time is desperately needed [2,3]. For that reason, this master thesis will explore the use of ultra-short voltage pulses (100ns) to achieve TDDB lifetime prediction. Such ultra-short pulses can be applied with a TLP (Transmission-line-pulsing) system, available in imec. The master thesis student will test the feasibility using TLP-pulses to predict oxide breakdown voltage and explore how "good" this new testing method compares to the state-of-the-art TDDB characterization. Depending on the findings, a hybrid measurement routine can be proposed together with the student where TLP and TDDB characterization methods complement each other. The master thesis requires a student with interest in /experience with measurement tools, computer programming and MOSFET characterization. Distribution of work is Literature Study (10%), measurements and measurements automatization (40%), data analysis and modeling (50%).

[1] Wikipedia, "TDDB", [2] Malobabic et al., Proc. Internat. Caribb. Conf. on Devices, circuits and systems, 2008 [3] Ille et al., EOS/ESD Symposium, 2006

Type of project: Thesis project

Degree: Master in Engineering majoring in nanoscience/nanotechnology, physics, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Geert Hellings (Geert.hellings@imec.be) and Ben Kaczer (ben.kaczer@imec.be).

Controlled transfer of two dimensional material

Two dimensional materials are promising candidates for integration in future electronic, (bio)sensing, photonic and even energy applications. The list of available 2D materials is very long and include transition metal dichalcogenides (e.g. MoS2, MoSe2, WS2...), graphene, phosphorene, h-BN... The range of interesting physical properties of these 2D materials includes high thermal conductivity, flexibility, tunable light absorption, superconductivity, high mobility... All these properties are combined with the ultimate thickness control that can be achieved with these 2D materials. As a result, van der Waals (hetero)structures are very interesting for future electronic applications. It is clear that a low 2D material defect density is required for the development of these electronic devices. The best synthetic 2D material quality is currently obtained during high temperatures growth processes (>>700 degrees). This high growth temperatures makes it practically impossible to directly deposit the 2D material at the desired location in a device. As a result, the transfer of these 2D materials seems unavoidable, while the knowledge to perform such a transfer process is currently very poor. A typical transfer process consist of the delamination of the 2D material from its growth substrate, followed by the lamination on a desired target substrate. As these 2D materials are only van der Waals bonded, it is immediately clear that such a pick and place process is already very challenging on its own. To complicate the transfer process further, the ultimate thickness scaling of these 2D materials makes them strongly influenced by their surroundings. Some of the materials are not only sensitive to doping by surrounding molecules, but are even very vulnerable to oxidation. This makes control over both top and bottom interface extremely important. Furthermore, the flexible nature of these materials make stress/strain control very important. On the contrary, one could use the sensitivity of these materials to dope them in a controlled way or even change its properties by varying the stress over the layer. In order to obtain this level of control, one has to gain much more fundamental insights in the behavior of these 2D materials when handling and laminating them on different materials. It is very clear that different challenges lie ahead to achieve a successful transfer. For example, one needs to understand how adhesion forces can be tuned to achieve a successful 2D material delamination from the growth substrate, but also a successful lamination on a target substrate. Since everything occurs at interfaces, experimental research is challenging and state-of-the-art characterization techniques will have to be used to achieve the necessary level of understanding. Heterogeneous 2D material stacking might be a possible way forward to control to a certain extend these 2D interfaces. The main focus of the thesis will be the fabrication of heterogeneously stacked 2D layers. Characterization techniques (AFM, SEM, Raman, XRD, XRR...) will be used during the course of the project.

Type of project: Thesis or internship project

Degree: Master in Science or Master in Engineering majoring in nanoscience/nanotechnology, physics, materials engineering, chemistry/chemical engineering

Responsible scientist(s):
For further information or for application, please contact Steven Brems (steven.brems@imec.be) and Ken Verguts (ken.verguts@imec.be).

High performance photonic grating couplers leveraging the small critical dimensions possible with advanced lithography

Grating couplers provide outstanding interconnectivity between large index contrast waveguides (silicon on insulator and silicon nitride platform) and fibers. Therefore, grating couplers are intensely investigated to optimize performance characteristics such as high coupling efficiency, polarization diversity or/and independency and reduced back-reflections. Among the various characteristics of grating couplers, reducing back-reflections becomes more

important for the integration of optoelectronic devices and minimizing instabilities and errors of interferometric devices. The back-reflections come from two major sources. One is the second order reflection of the grating coupler. It can be suppressed by setting the coupling angle between the fiber axis and grating coupler surface to a 10° tilt. The other is the Fresnel reflection at the boundary between the input waveguide and the grating trench area. Several methods of reducing the Fresnel reflection in the grating coupler have been proposed by many researchers such as a rib waveguide mode, a tilted elliptical grating coupler, an apodized grating coupler, a subwavelength structured grating, and asymmetric grating trenches. Recently asymmetric grating trenches for low back-reflections has been demonstrated by our group as shown in Fig. 1[1]. Therefore, we expect that combining nano-structures [2] (sub-wavelength structures including apodization) with the optimization of the asymmetric grating design will improve the characteristics of back reflections.

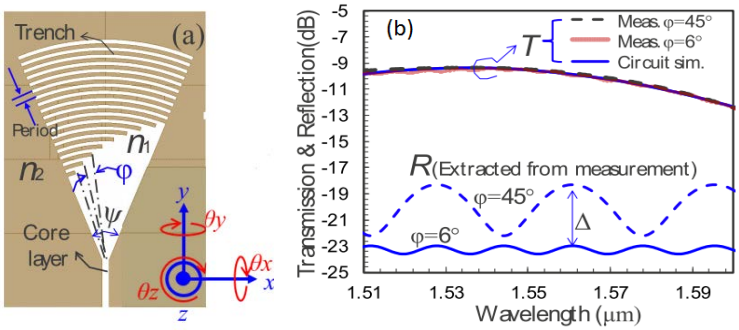


Fig.1. Example design of low back reflection grating coupler for communication-band[1].

(a) The design of asymmetric grating coupler when φ=6° and (b) its performance (transmission and reflection) comparison between asymmetric and conventional designs. Here conventional grating coupler is defined as φ=45°.

In this topic as a master thesis, the student can research and develop a high performance grating coupler with low back reflections for visible light coupling using the redesign of asymmetric grating coupler [1] and combining existing all techniques such as sub-wavelength structured grating with apodization technique. More emphasis is paid to use refractive index engineering with sub-wavelength structures [2] for the high performance of grating couplers.
The master student will study and make a performance thru this topic.

- Idea generation for a novel scheme of the high performance grating couplers.
- Basic / advanced scripting for FDTD simulations.
- Design skill for photonic devices using commercial simulation tool packages.
- Basic optics/photonics theory (silicon photonics, raytracing, waveguide optics, Gaussian optics).
- The target is a high performing, low back reflection grating in the visible.

Reference

[1] Song, Jeong Hwan, Bradley Snyder, Kristof Lodewijks, Roelof Jansen, and Xavier Rottenberg. "Grating Coupler Design for Reduced Back-Reflections." IEEE Photonics Technology Letters 30, no. 2 (2018): 217-220.
[2] Wang, Yun, Xu Wang, Jonas Flueckiger, Han Yun, Wei Shi, Richard Bojko, Nicolas AF Jaeger, and Lukas Chrostowski. "Focusing sub-wavelength grating couplers with low back reflections for rapid prototyping of silicon photonic circuits." Optics express 22, no. 17 (2014): 20652-20662.

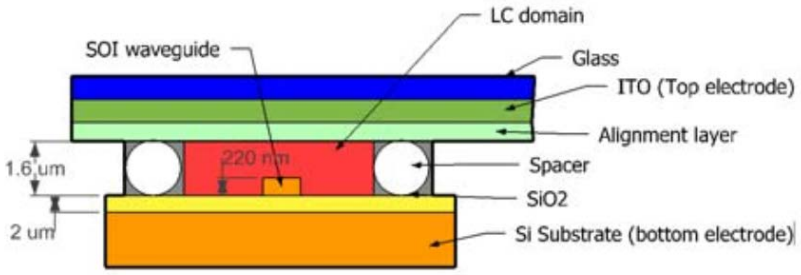
Type of project: Thesis project

Degree: Master majoring in physics, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Roelof Jansen (roelof.jansen@imec.be).

Development of a liquid crystal-based phase shifter for the SiN photonics platform

In the last 50 years, the successful integration of electronics on-chip led to performant and cheap integrated electronic circuits. More recently, a similar evolution started for optics, which has similarly been called integrated photonics. At first the well-established silicon technology was used to design integrated photonic circuits. However, silicon (Si) is not a suitable material for visible light since its bandgap is too small. Therefore a different material was necessary to make integrated photonic circuits for visible light, hereto silicon nitride (SiN) was considered as an on-chip waveguiding material. Unfortunately, this material is only useful for passive photonic circuits. In order to make reconfigurable photonic circuits an active component needs to be included in the platform.
In this master thesis we propose to design an electro-optic phase shifter for visible light by covering SiN waveguides with liquid crystals (LC). This will require selection of a suitable LC, fabrication of the devices, and measurement of your fabricated devices.



Example of a cross-section of a silicon photonics-based liquid crystal phase shifter.[1]

[1] N. Hattasan, W. D. Cort, J. Beeckman, K. Neyts, and R. Baets, "Tunable Silicon-on-Insulator based integrated optical filters with liquid crystal cladding," in 2009 IEEE LEOS Annual Meeting Conference Proceedings, 2009, pp. 189–190.

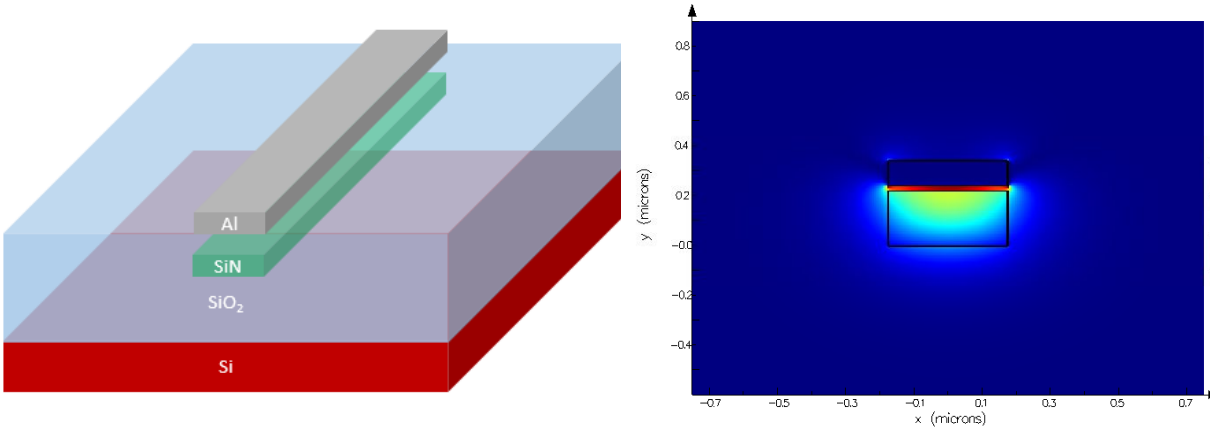
Type of project: Thesis project

Degree: Master in Science or Master in Engineering majoring in physics, electrotechnics/electrical engineering, materials engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Bruno Figeys (Bruno.Figeys@imec.be).

Hybrid plasmonic-photonic devices for silicon nitride integrated circuits

In recent years, imec has built a mature silicon nitride photonics platform for visible light applications. One of the many applications we focus on is biological sensing, a field in which there is also a lot of activity in plasmonic devices. Most conventional plasmonic materials such as gold and silver are not compatible with CMOS based processing in our pilot lines, but there are other plasmonic materials such as aluminum and copper are already part of this platform and allow to also target plasmonic applications. This thesis will focus on the design of hybrid plasmonic-photonic devices to be integrated in such platform. A typical example of such a component is a grating coupler that is used to couple light from an optical fiber into a propagating mode in the waveguide platform. In order to ensure that only the desired mode is coupled into the waveguide, such gratings could be equipped with a plasmonic filter that only allows one linear polarization state to be coupled, while rejecting all other polarizations. The work will focus on design and modelling of such components using state-of-the art commercial software packages, but also to propose test structures to verify the simulated results at a later stage.



Type of project: Thesis project

Duration: 6 months

Degree: Master in Science or Master in Engineering majoring in physics, electrotechnics/electrical engineering, materials engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Bruno Figeys (Bruno.Figeys@imec.be) and Kristof Lodewijks (Kristof.Lodewijks@imec.be).

Electrochemical deposition of CuNi alloys for chip microbump technology

A pressing issue in chip interconnection technology (multiple core chips) is the breakdown of microbumps over time. These microbumps are the physical and electrical connections between the chips. They consist out of copper stages on both chips which are typically soldered together by tin. Due to diffusion and electromigration, Cu and Sn form two intermetallic phases of which Cu3Sn induces microvoids at the Cu3Sn/Cu interface causing in turn breakdown of the microbump and therefore the whole chip. Chemical modelling shows that a CuNi alloy, with an approximate 9:1 Cu:Ni ratio, together with Sn doesn't form the Cu3Sn intermetallic compound thus tremendously improving the stability of the microbumps, and therefore the chip. By far the most feasible method to manufacture microbumps is galvanostatic (constant current) electrochemical deposition. However, electrochemical CuNi co-deposition from a single deposition bath requires current densities higher than the limiting current density of copper causing rough, uncontrolled growth of Cu. Existing CuNi baths are citrate based but citrates can corrupt other features of the chip manufacturing process.
So far, we have shown that the additive BTA has a tremendous potential for suppressing Cu2+ reduction and limiting rough Cu growth. However, if we want to deposit smooth CuNi alloys with a correct 9:1 ratio inside microstructures, we need to investigate additional additions of additives to the deposition bath to allow us to deposit smoother CuNi layers in a more controlled way. In this thesis, you will investigate the effect of typical plating additives for Nickel deposition for CuNi deposition and investigate their effect on the cupric ion reduction kinetics. Adding new components to a deposition bath requires an investigation of its effect/interference on the already present bath components and on the electrochemical parameters. Our goal is to develop an improved deposition bath for CuNi co-deposition by adding a new additive and defining a clear parameter window for which it doesn't interfere with other bath components and improves the smoothness and elemental composition of the deposit. For this work you will be trained in different techniques such as Rotating Disk Voltammetry, Chronopotentiometry, EDX and SEM. You will be challenged to think in creative and innovative ways.

Type of project: Thesis project

Degree: Master in Science or Master in Engineering majoring in chemistry/chemical engineering, materials engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Karel Haesevoets (Karel.Haesevoets@imec.be).

Ge(Si) multi quantum well based optoelectronic devices

Germanium (Ge) is a promising material for Silicon Photonics that is available in CMOS fabs. State-of-the-art electro-optic devices such as Ge photodetectors and modulators have been realized at imec and published. These devices are based on bulk Ge material. The performance of the Ge based modulator can be boosted dramatically, if similar device concepts are explored using Ge(Si) based multi quantum well (MQW) material system. Excitonic resonance peaks in quantum confined stark effect (QCSE) based absorption are the root cause for the performance boost in such a material system.
The student will be involved in designing basic structures and fabricating these devices at imec's clean-room. The intern will also characterize the structures opto-electrically, performing for example photocurrent-based experiments to analyze excitonic resonances and the QCSE behaviour. The intern will gain experience with optical lithography, RIE etching of Ge(Si) MQW stack, deposition of metal contacts for electro-optic experiments and polishing the waveguide facets after fabricating the devices. The intern will perform device characterization using scanning electron microscopy (SEM), optical characterization such as low temperature photoluminescence (low-T PL) spectroscopy and CV measurements to estimate the depletion width of the diode. These results will be used to calibrate the in-house developed model for a QCSE modulator.
The student will be guided by a team of optical and semiconductor physicists, material scientists and process engineers from the Optical Interconnects team at imec. As a result, students who have some exposure to the basics of semiconductor processing and/or solid state physics as a part of their curriculum or project(s) are highly encouraged to apply. Pre-requisites on optical physics, python or matlab would be beneficial but not essential.

Type of project: Internship, or thesis with internship project

Degree: Master in Science or Master in Engineering majoring in nanoscience/nanotechnology, physics, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Srinivasan Ashwyn (ashwyn.srinivasan@imec.be) and Marianna Pantouvaki (marianna.pantouvaki@imec.be).

Study of the kinetics of chemical reactions in nano-confined volumes

In semiconductor manufacturing, new generations of devices have entered the nano-world, with critical dimensions of the order of 10 nm. Many process steps are still performed using aqueous chemistries, e.g. wet etching of materials for patterning and wet cleaning of surfaces. New transistor geometries are vertical, with the generation of 1-D and 2-D nano-confined spaces (Fig. 1). The physico-chemical phenomena affecting the kinetics of chemical reactions in nano-confined volumes are not well understood. The only well-documented mechanism implies variations in concentrations of ions caused by surface charges and the overlap of electrostatic double layers (EDL). Differences in etch rates observed by Okuyama et al. (2015) and Vereecke et al. (2018) could be understood within that frame. However, changes in water properties, such as the increase in proton mobility, call for other mechanisms (Mawatari et al, 2014). In this project, we investigate the kinetics of chemical reactions in nano-channels/-holes with 1-D/2-D confinement. In a first part, the etching behavior of metallic layers covering the wall of nano-structures with varying dimensions will be studied (e.g. TiN using ammonia-hydrogen peroxide mixtures). The student will perform the wet etching tests, the data treatment of TEM (transmission electron microscopy) pictures generated by operators in the

pilot-line, and a kinetic analysis. Results will be compared to etch rates obtained on planar films with film thickness measured by ellipsometry. In a second part, the kinetics of a model click-reaction involving a SAM (self-assembled monolayer) deposited on the structures will be studied using ATR-FTIR (attenuated total reflection Fourier-transform IR spectroscopy). The method has already been developed and tested on nano-channels, where a rate decrease by a factor of 3 to 5 was observed. Here the student will prepare the ATR crystals (polishing), perform the FTIR tests using a home-build liquid cell, as well as the data treatment and interpretation. Kinetic studies will be complemented by the determination of the pH in the nano-structures by FTIR and of the surface potential by a streaming technique. The content of the student project will be adapted depending on the progress of our research.

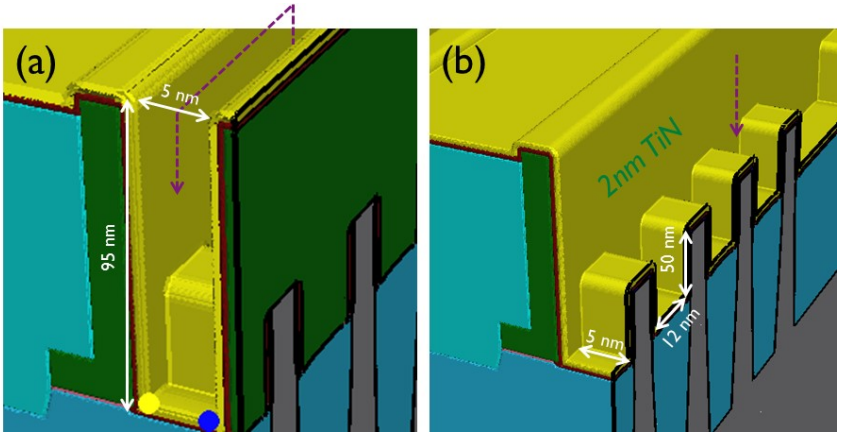


Figure 1. Cross-sections in a cartoon of a FINFET transistor after removal of the dummy gate (not to scale), showing (a) a nano-slit with 1-D confinement, (b) nano-holes with 2-D confinement.

Type of project: Internship or thesis project, or combination of both

Duration: 3 months

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in nanoscience/nanotechnology, chemistry/chemical engineering

Responsible scientist(s):
For further information or for application, please contact Guy Vereecke (Guy.vereecke@imec.be).

Explore process capabilities of state of the art etch reactors for advance device patterning

During the last decade an enormous growth of applications in the field of information, telecommunication and life sciences has occurred. To sustain this growth, the amount of integrated circuits (IC) in our daily life is augmenting, ranging from computers, tablets, mobile phones, TV's to cars, glasses, washing machines and healthcare. In 1971, Intel's 4004 processor held 2300 transistors; in 2013, Intel released its Quad-Core 4th generation i7 processor, with over 1.7 billion transistors. The continuous increment of pattern density with the aim of following Moore's law has brought many challenges to the integration processes involved in the manufacturing of integrated circuits. The semiconductor industry and R&D institutions are looking for solutions that allow the patterning of such tiny features with perfect geometrical shapes. With imec's state of the art etch tools, the student will explore the capabilities of such hardware which is able to etch few atomic layers. The question is: what is the process control and precision of atomic-layer etch?

1) The student will carry out 80% of experimental work and 20% with the aim to gain fundamental understanding on etch mechanisms. The goal is map plasma parameters (Gas flows, RF power, bias power, chuck temperature...) that influence material removal.
2) The student will get an in-house training on etch tool operation and working in a 300 mm clean room according to the safety rules. He/she will get familiar with measurement tools like: thickness measurement (ellipsometry), mass measurements, TOFSIMS, XRR. Next to that, he/she will get a basic training/understanding of plasma etch as he/she will operate the etch tool fully independently. Our etch literature library will be available to help him/her understanding the etch processes and key parameters that control the process.

Type of project: Thesis with internship project

Duration: 6 months

Degree: Master in Engineering Technology or Master in Science majoring in chemistry/chemical engineering, materials engineering, nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information or for application, please contact Efrain Altamirano Sanchez (Efrain.AltamiranoSanchez@imec.be) and Daniil Marinov (Daniil.Marinov@imec.be).

Experimental study of MOSFETs and TFETs with 2D flake materials

Since the fabrication of the first Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) in 1960, we have witnessed a tremendous increase in computational performance, driving worldwide technological innovation. This increase in performance was and is still possible by systematically downscaling the dimensions of the MOSFET, the basic building block of integrated circuits. Today, maintaining this scaling trend has become increasingly difficult, because the power consumption of the MOSFET can no longer be lowered sufficiently." [1] Therefore, the Tunneling Field-Effect Transistor (TFET) is a promising alternative to the MOSFET for low-power integrated circuits. "The carrier injection mechanism of the TFET is quantum mechanical Band-To-Band Tunneling (BTBT). This is accompanied by an energy filtering mechanism, which allows switching from the off-state to the on-state using a lower supply voltage than MOSFET, and hence reducing the power consumption of integrated circuits." [1]
This topic is about the experimental study of MOSFETs and TFETs made with 2D materials. The candidate will start with the fabrication of MOSFETs (figure 1) and TFETs (figure 2) fully encapsulated in hexagonal boron nitride. Then the candidate will proceed with the physical and electrical characterization of the devices and the interpretation of the electrical results. In the final stage, the candidate will decouple the different physical mechanisms occurring in the device. This topic offers a unique opportunity to get acquainted with the quantum mechanical BTBT mechanism and 2D semiconductors through hands-on experience, while making a contribution to the field of exploratory devices and logic downscaling.

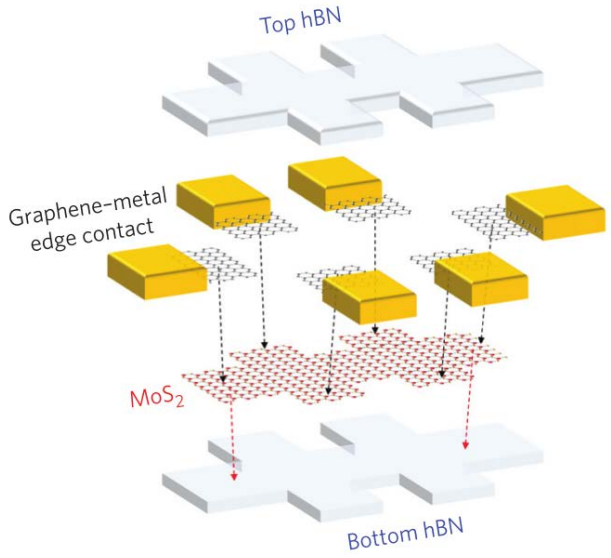


Figure 1: MOSFET with MoS2 channel encapsulated in hexagonal boron nitride, and graphene contacts. Image from [2].

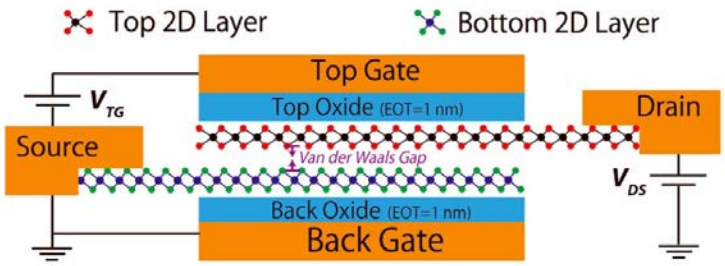


Figure 2: Schematic diagram of tunneling field effect transistor with 2D heterojunction materials. Image from [3].

This topic is very challenging and requires a full commitment. The candidate should have a strong background in Semiconductor Physics, Semiconductor Devices and Quantum mechanics, and sufficient dexterity for flake exfoliation and stacking. The candidate will be part of imec's "2D materials" team, and will enjoy the supervision by experts in fabrication and characterization of TFET devices. However, the candidate should have strong decision-making skills and should actively participate in project pathfinding. The candidate should read references [2-4] before applying for the topic.

[1] Q. Smets, PhD thesis (2016), https://lirias.kuleuven.be/bitstream/123456789/544428/1/thesis.pdf
[2] X. Cui et al., Nat. Nano. (2015), http://www.nature.com/doifinder/10.1038/nnano.2015.70
[3] D. Jena et al., Proc. IEEE (2013), http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6513300
[4] M. Li et al., JEDS (2015), http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7006653

Type of project: Internship or thesis project

Duration: minimum 6 months

Degree: Master in Science or Master in Engineering majoring in electrotechnics/electrical engineering, materials engineering, nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information or for application, please contact Quentin Smets (smetsq@imec.be).

II. Image Sensors and Vision Systems

There are currently no Master thesis/internship projects available in this research domain.

III. Silicon Photonics

Investigation of Cl based species on maximal dopand concentration of group IV epitaxial layers

Epitaxial growth of group IV materials is a well-known process and it is used at many different steps during the production of a wide range of semiconductor devices ranging from lasers to p-MOS FETs. Epitaxial Si is a base for the production of practically every chip. SiGe is responsible for success of both high frequency BICMOS and highly scaled CMOS transistors.
At present, most of the major semiconductor players produce chips on the fin FET technology at 14-16 nm technology node with 10 nm being around the corner. It is also often considered that devices at 7 and 5 nm or even smaller nodes will be based on group IV semiconductors (SiGe, Ge). SiGe and Ge, contrary to Si allow to improve electrical characteristics of pMOS transistors due to higher intrinsic holes mobility.
Although conventional growth of group IV materials on Si is well known, new device architectures (finFETs, gate all around FETs, nanowire FETs, etc.) impose very stringent requirements on composition, doping, thermal budget, etc. In many cases epitaxial material has to be grown at temperatures which are too low for conventional precursors used in the semiconductor industry (silane, dichlorosilane, germane) resulting in very low deposition rates. Increase of temperature often leads to changed devices geometry and loss of performance.
In order to solve mentioned above problems high order germanes and silanes receive lately considerable attention. Non selective processes based on such precursors have been developed and used for the production of GAA FinFet devices, electro absorption modulators, memory devices. The next step is to investigate possibilities for doping and selectivity in order to develop processes suitable for application on patterned wafers.
The aim of this work will be to study the epitaxial growth, doping and etch of SiGe using advanced precursors for epitaxy. The main focus will concern the growth kinetics, structural and electrical properties of the obtained layers. The candidate is expected to:

- focus on the epitaxial growth aspects and study the physics and chemistry involved in CVD of group IV materials using high-order silanes and germanes
- investigate epitaxial material quality, characterize defects and study their electrical activity
- learn and master such characterization techniques as X-ray diffraction, SEM,SIMS, etc.

Type of project: Internship or thesis project, or combination of both

Duration: 6 months

Degree: Master in Science or Master in Engineering majoring in chemistry/chemical engineering, materials engineering, nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information or for application, please contact Andriy Hikavyy (Andriy.Hikavyy@imec.be), Clement Porret (Clement.Porret@imec.be) and Roger Loo (Roger.Loo@imec.be).

Silicon photonics static process control and report automation

Silicon photonics technology has the advantage of tight light confinement that can be achieved in silicon waveguides, which can enable photonics devices of micrometer-sizes. In addition, silicon photonics can realize complex photonics circuits that can be produced using existing CMOS fab infrastructure on 200mm or 300mm wafers, providing cost-effective high-quality compact optical systems. Imec is playing a crucial role in the development of wafer-scale silicon photonics, and has already developed a state-of-the-art silicon photonics platform for high-speed optical interconnects.

We are looking for an enthousiastic, responsible intern to join our Photonics Integration Team. In this position, you will gain valuable insight about Silicon Photonics processing, and about challenges that need to be addressed to develop a stable platform. You will learn in detail about the Static Process Control for both inline (fabrication process quality monitoring) and End of Line (Electrical process quality) setup and optimization. You will become familiar with techniques that are being used to control variability in processing in an industrial fabrication environment, and you will learn to analyze and corellate inline and end-of-line data. Understanding the device physics and automation coding skills will be required to generate reports from available data that address specific topics. Your Key focus is to set up SPC process Charts and to setup automated reports.
Intern responsibilities :

- Setup and Clean the SPC Charts for Inline Process data
- Maintain SPC Charts for Electrical Test data
- Test Chip and Test Plan need to be systematized for multiple masks
- Examine the process history for different Silicon Photonics wafers/lots over time and clean up the graphs accordingly
- Develop coading for automated reporting system for lot tracking and process report

Type of project: Internship project

Degree: Master in Engineering Technology or Master in Science majoring in nanoscience/nanotechnology, electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Peter Verheyen (Peter.Verheyen@imec.be), Sadhishkumar Balakrishnan (Sadhishkumar.Balakrishnan@imec.be) and Marianna Pantouvaki (Marianna.Pantouvaki@imec.be).

Optical interface for alignment-tolerant silicon photonics packaging

In order to meet the requirements of high-speed communication bandwidth of future data centers, silicon photonic interconnects offer potential in mitigating bandwidth-power limitations of their electrical counterparts. The development of a highly efficient and compact interface between CMOS-compatible silicon photonics and polymer waveguides offers a promising approach towards 3D electro-optic integration. The aim of the project will be to develop a photonic chip-to-package substrate coupling interface for single-mode operation across O-band/C-band wavelengths of operation. The work involves understanding of the problem through simulations and cleanroom processing thereafter of photonic chips to achieve the goals of the required design. The student will obtain experience in optical design, semiconductor processing and measurements. A preliminary background of basic fundamentals in optics and integrated photonics is expected. Knowledge and some experience of cleanroom processing will be a plus.

Type of project: Thesis project

Degree: Master majoring in nanoscience/nanotechnology, electrotechnics/electrical engineering, physics

Responsible scientist(s):
For further information or for application, please contact Nivesh Mangal (nivesh.mangal@imec.be), Brad Snyder (Brad.snyder@imec.be) and Geert Van Steenberge (Geert.VanSteenberge@UGent.be).

Design and analysis of high-speed optical link using silicon photonics and FinFET technology

With the increase of bandwidth requirements for data centers and high-performance computing, optical interconnects are attracting an increasing interest for short-reach links. However, for optical interconnects to be adopted as a replacement for regular electrical connections, the performances have to be higher than its electrical counterpart while consuming less power. Silicon photonics technology is an excellent candidate for achieving these goals, and current optical components can operate at speed higher than 50Gbps. Using wavelength division multiplexing and/or complex modulation schemes, such as phase amplitude modulation, the bit-rate can further be increased to several hundreds of gigabits per second. Moreover, new types of optical components are in development aiming to reduce the power consumption of upcoming links while maintaining high speed.
In this topic the student will model optical links that are using imec's optical components and transceiver electronics based on advanced CMOS process nodes. System-level modeling will be done using Matlab/Python and Cadence/Lumerical software. With her/his model, the student will explore different architectures of optical interconnect links and evaluate them in terms of power consumption and performance.
Her/his work will involve cross-domain interactions from silicon photonics to circuit design and system-level analysis. The student will be guided by a team of experts in each of these fields and will have to opportunity to acquire some basic knowledge in silicon photonics, advanced CMOS circuit design to neural networks while also building a good understanding of optical communications and optical I/O interfaces.
Prerequisites in analog circuit design, Matlab, python, cadence would be beneficial but not essential.

Type of project: Thesis project

Degree: Master in Engineering majoring in nanoscience/nanotechnology, electrotechnics/electrical engineering, physics, computer science

Responsible scientist(s):
For further information or for application, please contact Nicolas Pantano (Nicolas.pantano@imec.be) and Dimitrios Velenis (Dimitrios.Velenis@imec.be).

IV. Thin-Film Flexible Electronics

3D TFT-based combined circuit and architecture exploration for cost and energy

The communication and compute component organisation in embedded systems are a major source of cost and energy. The use of cheaper and very low leakage TFT materials to replace silicon CMOS potentially allows to significantly improve on this. But we also want to exploit the growing potential of 3Dinterconnect technologies. In this MSc thesis we want to explore3D TFT-based combined circuit and architecture solutions which reduce especially the overall system cost and system energy consumption. We will focus especially on computing components like convolutional arrays and segmented bus and related communication blocks. Simulations will be performed based on available measurement data to calibrate the cost, energy and performance models. Profile: Strong interest in circuit and architecture exploration and simulation, basics of microelectronic technologies with emphasis on TFT and 3D interconnect schemes.

Type of project: Thesis project

Duration: 6 months

Degree: Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Kris Myny (kris.myny@imec.be) and Francky Catthoor (catthoor@imec.be).

Vertical channel oxide TFTs for low power and small foot-print device applications

This internship deals with thin-film transistors (TFTs) based on metal-oxide semiconductors. The technology is currently in use for future (flexible) displays and for tiny wireless devices connected to the internet of things. The advantages such as high uniformity, high electron mobility between 10 - 50 cm2/V·s, and fabrication at low temperatures of metal-oxide TFTs are promising for next-generation high-resolution backplanes for displays and low power circuits. For further improvement of resolution (8k4k) in displays and other low power applications, the size of TFT should be minimized. Currently in use, staggered bottom gate (back-channel-etch & etch-stop-layer) and coplanar top gate (self-aligned) TFT structures have large foot prints with high power consumption. In general, reducing the driving voltages or foot-print can be accomplished by reducing the thickness of gate insulator and dimensions of channel (done by lithography), respectively. Vertical channel TFT structure is another approach to reduce the foot-print and driving voltage. In this structure, the controlled channel length defined by thickness of spacer between source and drain will result in uniform on current in comparison to channel defined by lithography on large areas. The objective of this master thesis/internship is to integrate vertical oxide TFTs on glass/polyimide substrate. It's an experimental study with a substantial hand-on work in the cleanroom. The activity will also include electrical characterization of the manufactured TFT devices. From the results a conclusion need to be drawn on the device structure, interface issues and stack materials.

Type of project: Thesis or internship project

Duration: 6 months

Degree: Master in Engineering Technology or Master in Science majoring in electrotechnics/electrical engineering, materials engineering, nanoscience & nanotechnology, physics

Responsible scientist(s):
For further information or for application, please contact Manoj Nag (manoj.nag@imec.be).

High-k gate dielectrics (HfO2 & Al2O3) to boost the performance of a-IGZO thin-film transistors

This internship deals with an emerging class of semiconductor devices – thin-film transistors (TFTs) based on complex metal-oxide semiconductors – a hot topic in the research community. Oxide transistors are pretty different from traditional silicon CMOS, they can be manufactured very quickly, on very large substrates, and at relatively low cost. It's an interesting candidate technology for future (flexible) displays and for tiny wireless devices connected to the internet of things. Significant investments in this technology are made by the industry already today. Examples of advanced metal-oxides from latest research publications are zinc tin oxide (ZTO), gallium doped zinc oxide (GZO), indium zinc oxide (IZO), and indium gallium zinc oxide (IGZO). This internship will focus on the latter material, amorphous IGZO, it shows a good device performance and promising industrial compatibility. Researchers reported remarkable achievements with this oxide material. You will take it to the next level by focusing on improvements of the gate insulator layer. Common technologies use conventional low-k materials as gate insulators, a very common example is SiO2. Relatively low capacitance of such low-k layers limits the ultimate transistor performance. This internship aims to unlock this limitation by introducing new high-κ materials for gate insulators. You will work with Al2O3, ZrO2 and HfO2 to create TFT devices with reduced electron tunneling, large gate capacitance, and high drive currents. The higher dielectric constant allows for comparable TFT performance at a lower operation voltage. The objective of this master thesis/internship is to investigate the use of high-k materials in imec's state-of-the-art IGZO TFT technology. It's an experimental study with a substantial hand-on work in the cleanroom. The new high-k layers are deposited by atomic layer deposition, previous experience with ALD techniques is an asset. The activity will also include electrical characterization of the manufactured TFT devices. From the results a conclusion need to be drawn on the device structure, interface issues and stack materials.

Type of project: Thesis or internship project

Duration: 6 months

Degree: Master in Engineering Technology or Master in Science majoring in electrotechnics/electrical engineering, materials engineering, nanoscience & nanotechnology, physics

Responsible scientist(s):
For further information or for application, please contact Manoj Nag (manoj.nag@imec.be).

PZT sol-gel process development on large area substrate for piezoelectric actuators

Traditional microphone units focus on human perceptible sound waves (between 20 Hz and 20 kHz). Acoustic development also includes the ultrasound region, compromising the frequencies above the detection limit of the human ear (from 20 kHz to several GHz). These sound waves can be used for a wide variety of applications, including medical imaging, therapeutic treatment, non-destructive testing and position localization of objects. Nowadays, the ultrasonic transducer and sensor technology is largely based on rigid bulk piezoelectric ceramic materials, such as lead zirconate titanate or barium titanate. Classical techniques to grow such ceramic materials require high process temperature and dedicated substrates. Although this is a mature technology for discrete passive components, offering a reasonably wide bandwidth and sensitivity, it is not amenable to machine large two-dimensional (2D) transducer arrays. Monolithical integration with other electronic components such as signal processing electronics is hardly possible. To waive this problem, development of non-traditional techniques such as sol-gel based deposition is needed. This is crucial for applications where large arrays are needed and for which a high level of integration is clear a must. In the past years, imec has led the development of novel technologies that promise to meet all requirements of future micro-sound systems. The Large Area Electronics (LAE) and System in Foil (SiF) technology platforms allow

to produce passive and active components in thin-film frameworks with world-leading performance and in flexible form factors. Further, preliminary demonstrations of ultrasound components monolithically integrated with their drive and readout electronics are emerging. These developments support the perspective to develop multimodal ultrasonic sensing and actuating skins. The purpose of this internship is to develop novel processes for the next generation ultrasound transducers on large area technology using piezoelectric ceramic material deposited with a sol-gel based technique. The student will invent the process scheme and analyze the resulting thin-film, to investigate the compatibility with imec's thin-film piezoelectric devices. Depending on the interest of student, this can be extended to the full integration of the piezoelectric devices and analysis there-off in comparison to existing ones.

Type of project: Thesis or internship project, or combination of both

Duration: 6 months

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in electrotechnics/electrical engineering, materials engineering, nanoscience & nanotechnology, chemistry/chemical engineering

Responsible scientist(s):
For further information or for application, please contact Yongbin Jeong (Yongbin.Jeong@imec.be) and David Cheyns (David.cheyns@imec.be).

Stack optimization of infrared thin-film photodetectors

Most modern infrared photodiode arrays combine a silicon based backplane with an infrared absorbing material. These thick substrates are flip-bonded to the backplanes, which limits the pixel resolution. Processing directly on top of a silicone backplane will increase the pixel density and decreases the production cost. At the same time, this solution will create options to fabricate flexible photodetectors, processing the infrared materials on sheets in combination with flexible electronics. In the recent years, colloidal quantum dots (QDs) received an increasing amount of attention due to their opto-electronic properties, with applications in light-emitting diodes and photovoltaics. Once the size of a nanoparticle reaches the exciton Bohr radius, quantum confinement effects will affect both the light absorption and emission spectrum of the material. By starting from a bulk material with infrared absorbing properties, one can obtain visible or infrared absorbing quantum dots. The quantum dots are typically surrounded by organic ligands that stabilize the material. The material can be made soluble by selecting the correct ligand. Moreover, these ligands can limit the large surface recombination inherent to the small quantum dots. The focus of this internship will be the optimization of the photodiode stack by the use of a variety of electron (ETL) and hole (HTL) transport layers as well as by the use of different ligand strategies for the passivation of the QDs. Through this study a better understanding of the p-n junction of the photodiodes will be obtained, while proper energy band engineering will be crucial for the achievement of higher performance. The findings of this research will be then applied into the realization of photodetector devices successfully on glass and on silicon and these devices will be electrically characterized. The student will receive training on the relevant processing and characterization tools. After a short introduction to the facilities, an independent investigation is expected with the focus on short-term research goals.

Type of project: Thesis or internship project, or combination of both

Duration: 6 months

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in electrotechnics/electrical engineering, materials engineering, nanoscience & nanotechnology, chemistry/chemical engineering

Responsible scientist(s):
For further information for application, please contact Epimitheas Georgitzikis (Epimitheas.Georgitzikis@imec.be), David Cheyns (David.cheyns@imec.be) and Pawel Malinowski (Pawel.malinowski@imec.be).

Low-temperature polysilicon TFT virtual design library

Thin-film transistors (TFTs) are currently the dominant technology for in-pixel switches in flat-panel displays. The current trends drives TFT devices to deliver more complex functions than simply switching, like in integrated TFT-based row selector circuit enabling to reduce the bezels. TFT circuits can be fabricated on large substrates, thereby creating very thin, lightweight and ultra-flexible electronics. A flexible TFT-based microprocessor and a near-field communication (NFC) tag have already been demonstrated. The mainstream high-end TFT technologies are based
You, as a student, will enable the creation of a virtual library for both technologies, comprising of amongst others a standard cell library and TFT-models for Spice simulation. Such a virtual design library will be used to predict the outcome of certain design and technology choices and is therefore an important asset to assist our design and technology team.
You will be asked to report on the results and present your progress to the group.
You have the opportunity to work in a world-class design group in thin-film electronics, with the prospect of your results being used for the years to come.
Requirements:

- Self-motivated, inquisitive and independent
- Experience in Linux and Cadence
- Capable of writing clear reports

Type of project: Internship project

Duration: 6 months

Degree: Master majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information for application, please contact Kris Myny (kris.myny@imec.be).

Design and characterization of in-panel charge-sense amplifier for sensor array readout

Thin-film transistors (TFTs) are currently the dominant technology for in-pixel switches in flat-panel displays. The current trends drives TFT devices to deliver more complex functions than simply switching, like in integrated TFT-based row selector circuit enabling to reduce the bezels. TFT circuits can be fabricated on large substrates, thereby creating very thin, lightweight and ultra-flexible electronics. A flexible TFT-based microprocessor and a near-field communication (NFC) tag have already been demonstrated. Also the field of analog electronics based on TFT-technologies is maturing.
Analog signal conversion based on In-Ga-Zn-O TFTs can be implemented in fingerprint sensor arrays for direct integration on mobile AMOLED displays. This application case can benefit from an in-panel integrated charge-sense amplifier (CSA) combined to multiplexers reducing drastically the number of connections towards off-panel electronics.
You, as a student, will incrementally improve the design and layout of amplifiers and characterize the fabricated samples in an lab environment. Final target is to integrate the CSA with sensor arrays and characterize in real environment the system.
You will be asked to report on the results and present your progress to the group.

You have the opportunity to work in a world-class design group in thin-film electronics, with the prospect of your results being used for the years to come.
Requirements:

- Self-motivated, inquisitive and independent
- Experience in Linux and Cadence
- Capable to work in the lab
- Capable of writing clear reports

Type of project: Internship project

Duration: 6 months

Degree: Master majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information for application, please contact Kris Myny (kris.myny@imec.be) and Nikolas Papadopoulos (Nikolas.Papadopoulos@imec.be).

Research of ESD protection for the TFT technology

Thin-film transistors (TFTs) are currently the dominant technology for in-pixel switches in flat-panel displays. The current trends drives TFT devices to deliver more complex functions than simply switching, like in integrated TFT-based row selector circuit enabling to reduce the bezels. TFT circuits can be fabricated on large substrates, thereby creating very thin, lightweight and ultra-flexible electronics. A flexible TFT-based microprocessor and a near-field communication (NFC) tag have already been demonstrated. A missing link for TFT-applications is a better Electrostatic Discharge (ESD) protection circuit.
Every integrated circuit needs protection from the outside world before it becomes a product on its own. The internship candidate will join a team of imec researchers investigating solutions for ESD protection in the TFT technology. This investigation includes design, measurements, characterization, optimization of existing solutions and development of new ones. The goal of this internship is to make a scientific advance in the field of ESD for TFT technology and specifically for displays.
We are expecting a candidate who has a background in electrical engineering and is comfortable with working on multi-disciplinary topics. Knowledge of ESD, TFT, device/circuit characterization, modeling and design would be very welcome. A good team spirit is a must.

Type of project: Internship project

Duration: 3 months

Degree: Master majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information for application, please contact Kris Myny (kris.myny@imec.be), Marko Simicic (Marko.Simicic@imec.be) and Shih-Hung Chen (Shih-Hung.Chen@imec.be).

V. Life Sciences

Nano-scale field effect transistor for biomolecule sensing

With significant progress in CMOS process technology, we are now able to manufacture nano-scale Field-Effect Transistors (FETs) down to 7 nm. This has opened doors not just for better computing but also for areas like bio-sensing for proteins and DNA. An important innovation lies in large-scale integration of nanoscale transistors for analyzing biological systems, which could provide for massive parallelization and deliver a more complete view of a biological system at a reasonable cost. However, there are several challenges open that still need to be tackled to achieve such a large-scale bio-electronic sensor chip. In this master thesis, the student will investigate nano-sized field effect transistors for their ability to sense bio-molecules in electrolytic environments and try to understand the effect of surface functionalization on bio-sensing. In order to capture the target biomolecules on the FET, the surface of the transistor needs to be functionalized with special molecules that can bind with the target biomolecules floating around in the electrolyte solution. This surface functionalization can influence the bio-sensing ability of the FET, which is important if we want to achieve a low Limit of Detection (LOD). During the master thesis, these sensors will be characterized in detail to understand their behavior for different types and methods of surface functionalization. The student will also work on analyzing the noise contribution of the functionalization and the effect of the electrolytic environment. The thesis will involve working in the cleanroom, bio-chemistry labs and on electrical characterization tools. Molecular sensitivity and the potential of obtaining FET-based single molecule sensors will also be investigated.

Type of project: Internship or thesis project, or combination of both

Duration: 6 months

Degree: Master in Science or Master in Engineering majoring in electrotechnics/electrical engineering, chemistry/chemical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information for application, please contact Mihir Gupta (mihir.gupta@imec.be) and Koen Martens (koen.martens@imec.be).

Cell sorting and characterization for cancer cell therapy applications

High throughput cell sorting is increasingly important for precision medicine nowadays. On one hand, precisely sorted cells (e.g. cancer cells) are of important diagnostic value. They carry unique genomic and proteomic information, unique for the disease and patient. Once analyzed after sorting, e.g. by gene sequencing, the information can be used to create a better understanding of the disease at hand and subsequently prescribe personalized treatment. On the other hand, the sorted cells themselves could be used as a treatment. In recent years, adaptive cell immunotherapy turned out to be a groundbreaking method for fatal disease treatment such as cancer and AIDS. In this method, immune cells (T-cells) from the patient are sorted and genetically engineered to attack malignant cells. To further boost this medical development, Imec is developing a high throughput cell sorting platform using a micro bubble jet flow technique. The rapid jet flow is capable of sorting single cells within a few tens of micro seconds. The speed and scalability is promising for high throughput clinical cell sorting applications supporting the growing use of cell therapy. This master thesis will focus on assessing the impact of high speed microfluidic flow and rapid jet flow on T-cell viability, cytotoxicity and activation potential. Different subtypes of T-cells will be sorted using the existing cell sorting platform based on multiple sorting parameters. Subsequently, the sorted cells will be evaluated in terms of viability in cell culture and T-cell activation assays. Further, gene expression analysis can be investigated using micro array analysis or next generation sequencing. The massive data generated using this technology will be analyzed statistically to correlate various physical sorting parameters to the possible influence to

cell metabolism, viability or reactive expression of certain markers. The technical work will consist of 10% time on literature study, 30% on cell sorting, 30% on molecular sample preparation and 30% on data analysis.

Type of project: Thesis project

Degree: Master in Engineering Technology or Master in Science majoring in chemistry/chemical engineering, nanoscience/nanotechnology, bioscience engineering

Responsible scientist(s):
For further information for application, please contact Sarah Libbrecht (Sarah.Libbrecht@imec.be).

Building a microfluidic network for multiplex DNA amplification

Microfluidics is essential to realize fully automatic Lab-on-a-chip devices. In this thesis, student will design and fabricate a microfluidic device that has well-controlled surface hydrophilicities. The application goal is to find an scalable and autonomous solution for multiplex DNA amplification on chip, so that tedious pipetting steps of various reagents and samples can be replaced by automatic spotting and liquid transfer. The student will also learn to characterize the devices using microscopy, learn to perform DNA amplification on chip using polymerase chain reaction (PCR) method, and eventually demonstrate multiplex PCR on his/her fabricated devices.
The study will consist of 10% literature study, 45% fabrication, and 45% measurement.

Type of project: Thesis project

Degree: Master majoring in bioscience engineering, electrotechnics/electrical engineering, physics, nanoscience/nanotechnology, chemistry/chemical engineering

Responsible scientist(s):
For further information for application, please contact Lei Zhang (Lei.Zhang@imec.be) and John OCallaghan (John. OCallaghan@imec.be).

Photonic read out of waveguide integrated nanopores

DNA mapping and sequencing is seeing huge improvements through the use of nanopores, with the technology already being applied such as the Oxford nanopore systems. It's being used as a research tool for biologist as well as in the field in Africa and even by NASA.
However nanopore DNA sensing, especially electric has intrinsic challenges. These challenges entail, weak output signals, parallelization, high sensitivity to external factors (EM-interference) and "slow" throughput speeds. In this project we'll focus on a new emerging techniques, instead of measuring electronically we'll measure the signals optically. Sensing optically has the advantage that it has a spectrally flat noise spectrum, is not affected by electromagnetic fields and can be much more energy efficient. For the photonic sensor an initial design has already been made, taking fabrication limitations into account. Using fluorescent labels to tag DNA string is possible to accurately map DNA translocating through the photonic nanopore. This new sensor would allow for faster and cheaper DNA mapping and possibly sequencing. We expect this technology will have a direct impact on point of care biomedical research, diagnostics and precision medicine.
We expect a candidate student who has interests on and is self-motivated for Biophotonics with nanopore sensing, as well as microfluidics. The work contains photonic device characterizations, biophysics experiments, data analysis, and validations of the results.

Type of project: Thesis project

Duration: 6 months

Degree: Master in Science or Master in Engineering majoring in electrotechnics/electrical engineering, physics, nanoscience/nanotechnology

Responsible scientist(s):
For further information for application, please contact Chang Chen (Chang.Chen@imec.be), Pol Van Dorpe (Pol.VanDorpe@imec.be) and Bob van de Voort (Bob.vandeVoort@imec.be).

Simulation of nanopore transistors

With ever more advanced manufacturing techniques, many applications of semiconductors in the life sciences have emerged with devices capable of measuring at molecular sensitivities. One such promising application is the integration of nanopore technology with nanoscale transistors. This so-called nanopore transistor consists of a charged carrier channel surrounding a hole that allows macromolecules such as DNA to pass through it. The molecule affects the transport properties within the transistor channel by shifting the electric potential in the pore which in turn allows its identification. This concept could lead to a broad range of applications which even includes the next generation of DNA sequencers. At imec we aim to develop nanopore transistors at scale for the multi-billion dollar life science market. However, many challenges lie ahead which make the exploration of possible designs with numerical simulations essential. For this purpose we use an amalgamation of several software tools as well as our own developments since no off-the-shelf solutions exist. The successful candidate would use our toolchain to simulate various designs and compare their practical viability. Due to the interdisciplinary nature of this work, the experimental status of our toolchain, and the time constraints of a master's thesis, we require the successful candidate to be a physicist, electrical engineer, computational engineer, or similar with experience in at least one of the following fields: numerical solution of partial differential equations, semiconductor device physics, and/or nanofluidics. Some familiarity with programming and with using GNU/Linux is a plus. Since this thesis presents a challenge at the intersection of different fields of research, we strongly advise any candidate to take part in an interview to ensure that the qualifications are met.

Type of project: Thesis or internship project

Duration: 6 months

Degree: Master in Science or Master in Engineering majoring in electrotechnics/electrical engineering, physics, nanoscience/nanotechnology, computer science

Responsible scientist(s):
For further information for application, please contact Dino Ruic (Dino.ruic@imec.be) and Pol Van Dorpe (Pol.VanDorpe@imec.be).

CMOS compatible nanopore field-effect transistors

After decades of developments, nanopore-based sensing technology has made the step from fundamental research to applications. In the last few years nanopore sensors have been shown to count, detect, and identify nano-objects. A recent commercial example is the MinION from Oxford Nanopore Technologies Ltd, which has been used for in-field analysis of Ebola in Africa as well as whole genome sequencing in the International Space Station. More excitingly, new nanopore technologies keep on springing up all over the world.
At imec, we are working on combining the two smallest artificial solid-state devices: nanopores and state-of-the-art transistors. This will lead to the creation of an integrated nanopore field-effect transistor sensor. In this project, the focus is on learning the fundamental features and practical sensing capabilities of such new devices. The work contains both device characterizations and biosensing experiments carried out in our life lab. We expect a candidate student who is curious about watching the nanoworld through ECG like pulses, and is self-motivated for exploring a new field.

Type of project: Thesis or internship project

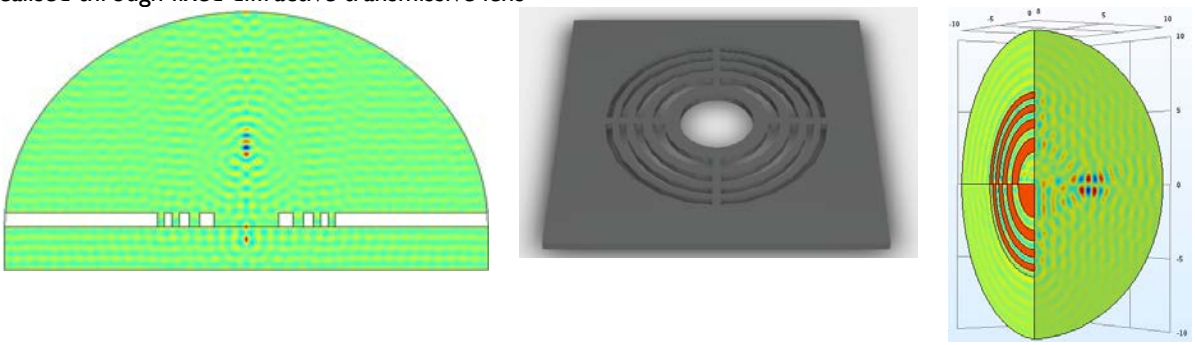
Duration: 6 months

Degree: Master in Science or Master in Engineering majoring in electrotechnics/electrical engineering, physics, nanoscience/nanotechnology

Responsible scientist(s):
For further information for application, please contact Chang Chen (chang.chen@imec.be) and Pol Van Dorpe (Pol.VanDorpe@imec.be).

Ultrasound holography using tunable acoustic lens

Acoustic imaging relies on the production and detection of controlled acoustic wave fronts. Emergent acoustic technologies allow nowadays to define large 2D arrays of high frequency ultrasound transducers, thus enabling imaging qualities never seen before. However, these new systems rely on expensive and complex RF-CMOS beam forming drive and readout circuits still under development. Indeed, generating precise phase shifts for millions of transducers is a task never encountered before.
An alternative to this RF-CMOS-based beam forming approach is to use simple plane-wave source or detector and retrieve to tunable lenses (transmissive or reflective) for wave front shaping. These lenses are reset through the application of DC-signals and thus do not require the development of complex RF-CMOS circuitry.
In this master thesis, we will investigate an acoustic tunable lens for ultrasound holography. Based on electromechanical and acoustic simulations, we will first define the acoustic beam-forming technique and acoustic/mechanical specification of the tunable lens and its cartesian set of acoustic actuator pixels to efficiently focus the ultrasound signal on specific location. Then we will implement the simulation results with an existing pMUT platform.
Simulation of acoustic reflective focusing; 3D printed fixed acoustic zone plate; simulation of acoustic tweezer realised through fixed diffractive transmissive lens



Simulation of acoustic reflective focusing; 3D printed fixed acoustic zone plate; simulation of acoustic tweezer realised through fixed diffractive transmissive lens

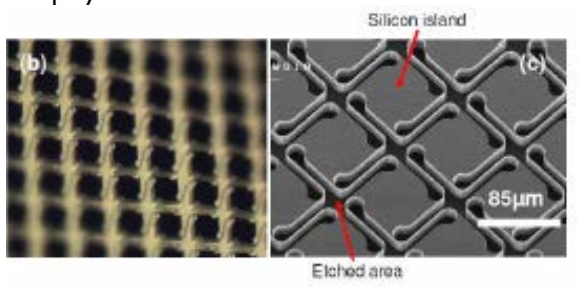
Type of project: Thesis project

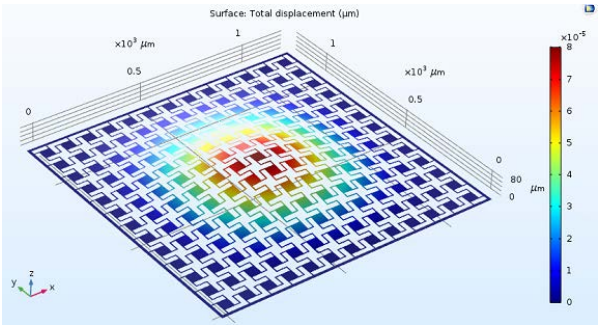
Degree: Master in Science or Master in Engineering majoring in bioscience engineering, electrotechnics/electrical engineering, materials engineering, mechanical engineering, physics, nanoscience/nanotechnology

Responsible scientist(s):
For further information for application, please contact Chih-Hsien Huang (Chih.Hsien.Huang@imec.be) and Xavier Rottenberg (Xavier.Rottenberg@imec.be).

Mechanical design of Kirigami structures for brain cell sensing

Recording electrical signals from the brain is of great interest to neuroscientists. Silicon promises great potential to implement electrode arrays to aid this recording. But tissues such as the brain are soft. To match the compliance of brain tissue, ideally the sensor array would be compliant. The goal of this master thesis is to optimize a thin mechanical sheet made in Silicon to maximize its flexibility and compatibility with the brain cells/tissue. The work will be performed by simulating the mechanics in Comsol software. The first step will be to design the periodic pattern to increase the total compliance of the sheet. Then we will investigate more complex structures that could be deployed in 3D.





S. Xu et al, Assembly of Micro/Nanomaterials into Complex, Three-dimensional Architectures by Compressive Buckling, Science, 347, 154 (2015)

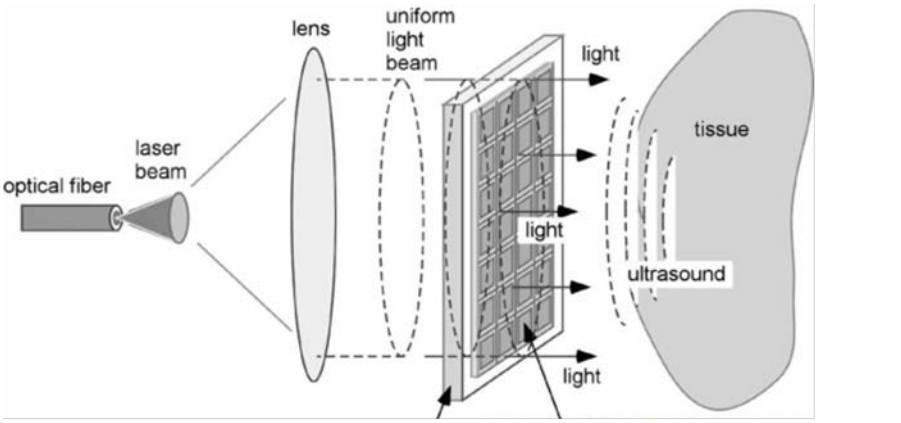
Type of project: Thesis or internship project

Degree: Master in Engineering majoring in electrotechnics/electrical engineering, mechanical engineering, physics

Responsible scientist(s):
For further information for application, please contact Veronique Rochus (Veronique.Rochus@imec.be) and Dries Braeken (Dries.Braeken@imec.be).

PhotoAcoustic imaging set-up

The goal of this work is to develop an integrated photo-acoustic imaging system. Photoacoustic imaging is a biomedical imaging modality based on the photoacoustic effect. Laser pulses are delivered into biological tissues. Part of the energy is absorbed and converted into heat, leading to transient thermoelastic expansion and thus ultrasonic emission. The generated ultrasonic waves are detected by ultrasound transducers and then analyzed to produce images. To improve the image quality and the form factor of the system, ultra-sensitive sensors and large array of small ultrasound transducers are required.
Imec is working on improving the performance of these ultrasound sensors by designing and implementing new ultrasound microphones. The work in this master thesis is to use these new sensors and build a photo-acoustic imaging set-up in order to evaluate the full system performance.



Type of project: Thesis project

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in bioscience engineering, electrotechnics/electrical engineering, mechanical engineering, physics, nanoscience/nanotechnology

Responsible scientist(s):
For further information for application, please contact Veronique Rochus (Veronique.Rochus@imec.be) and Xavier Rottenberg (xavier.rottenberg@imec.be).

VI. Wearables

Interface circuits for physically unclonable functions

Physically Unclonable Functions (PUF) are an emerging class of primitives for authentication and key generation in low-cost hardware security applications. They are based on the physical characteristics of an integrated circuit, whereby random variations occurring in the manufacturing of semiconductor devices are exploited to generate and store a unique key. The PUF cells are typically implemented with simple circuits, thus providing the potential for ultra low-power and small chip area consumption, and provide a low-cost alternative to solutions based on traditional digital memories, such as non-volatile memories (e.g. EEPROMs) or battery-backed SRAMs.
The proposed topic, concerns the design of the interface circuits necessary to generate and readout of a novel CMOS-based PUF relying on electrical breakdown for key generation and storage. The design will be implemented in an advanced CMOS node (22nm), and will be targeting application in next generation neural interfaces and wearable-health ICs. This work will involve the complete circuit design cycle, from specs definition to design and validation using EAD simulations, to layout of the designed circuits.
Required skills: Analog circuit analysis and IC design (at least basics). Software skills: Cadence Virtuoso, Matlab.

Type of project: Internship or thesis project, or combination of both

Degree: Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information for application, please contact Marco Ballini (marco.ballini@imec.be).

Unobtrusive measurement of capacitive electrocardiography (ECG) and bioimpedance (BIOZ) in automotive environment

The proposed thesis topic concerns the integration of the latest electronic system for capacitive acquisition of ECG and BIOZ into an automotive environment (i.e. car seat). This will involve both integration in terms of hardware, as well as firmware, and signal acquisition and low-level signal processing in Matlab.
The work also includes evaluation of the signal acquisition using the realized system under real-life conditions. Where appropriate, recommendations for modifications or additions to the electronic circuits or any other part of the system may be proposed and potentially be implemented.
Based on the acquired experimental data the student may also propose improvements to algorithms for handling motion artifacts based on the validation of imec's current algorithms under development, especially with a focus on real-life environment measurements. These validations and proposed improvements will be using the auxiliary signals that are currently being measured by imec's capacitive system (capacitive impedance, acceleration in 3 dimensions, and angular velocity in 3 dimensions from each electrode) and the adaptive robustness, artifact handling, and artifact reduction algorithms developed until now.
Skills required: test and measurement skills, experience using Matlab, at least basic mixed signal (analog and digital) electronic circuit knowledge, at least basic experience with embedded microcontroller firmware programming in C

Type of project: Internship project, or thesis with internship project

Duration: 5 months fulltime (6-9 months preferred)

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information for application, please contact Tom Torfs (tom.torfs@imec.be).

Wireless power transfer for deep implants

Recent years have seen a huge increase in advanced tools for remote health monitoring. Among other, a number of wearable devices have emerged in various form factors that can accurately and reliably measure important vital signs. A lot of research has focused on improving the reliability and quality of the sensing while at the same time multi-modal sensing resulted in unprecented levels of medically relevant diagnostic information. A lot of focus has gone on reducing power levels, while increasing the signal quality and diagnostic information. At the same time, a lot of research focused on providing all this in ever smaller form factor to make the technology as unobtrusive as possible. While wearable health technology is great and holds a lot of promise, a logical next step in this evolution is moving inside the body. More recently a shift can be witnessed towards research into advanced implantable devices that can be implanted via minimally invasive procedures. Examples include ingestibles, injectables, endoscopically implanted devices and subcutaneous implants. Imec is launching a major research effort into such advanced medical implant devices. One of the key problems here is off course power delivery. While batteries are in principle possible, they certainly are not desired due to a number of severe limitations (toxicity, patient safety and size/volume). Hence wireless power transfer is an interesting technology for these applications. In this internship we are looking for a good master's student with background in electrical engineering to tackle this major hurdle in this field. In this area, inductively coupled devices are the most prevalent, but they rely on fairly large coils. Furthermore those coils need to be properly aligned with the external coil. Another option is RF-based wireless power harvesting. In this internship we will explore what the most optimal technique for transferring power to deep implants is considering area/volume

constraints. We want to explore how small such implants can be made, while still being able to harvest enough power inside the human body.
The student is expected to research the most optimal technology and carrier frequency specifically for small antennas placed deep in the human body. The student must consider tissue absorption, antenna sizes and develop a suitable link budget. Once this study has completed, the student will be tasked to design custom integrated circuits for the implant side including rectifiers, self-starting boost circuits and potentially DC-DC converters. If time permits, the student will get the chance to also do the IC layout of the blocks designed which can be taped out and measured. Skills required: good knowledge of analog IC design; basic familiarity with Cadence and Spectre; basic familiarity with numerical analysis software like Matlab; basic knowledge about antenna design and properties.

Type of project: Internship or thesis project, or combination of both

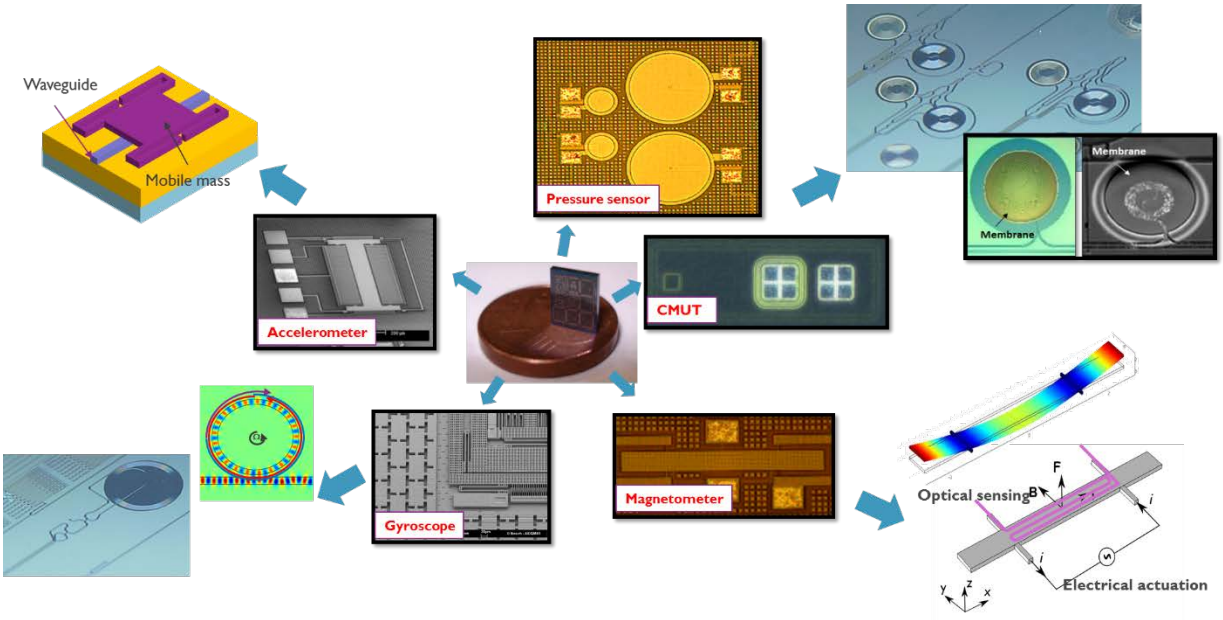
Degree: Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information for application, please contact Didac Gomez (Didac.GomezSalinas@imec.be).

Design of an optical IMU system

Global Positioning System (GPS) is the most common way for navigation. However, it needs a direct line of sight to a satellite, which is not applicable inside buildings or tunnel. An Inertia Measurement Unit (IMU) allows the unit keep track of positional changes when GPS-signals are unavailable. An IMU consists of three types of triaxial sensors (accelerometer, gyroscope and magnetometer) and uses a dead reckoning technique to calculate current position and velocity relative to an initial reference frame (before losing line-of-sight with satellites). IMU's are also used in the consumer industry in products such as smart phones, fitness trackers, drones and gaming motion controllers.

MEMS IMU systems have been demonstrated in the past at imec using piezo or capacitive read-out. The topic of this project is to replace the MEMS IMU components by optical sensing components. Micro-Opto-Mechanical Pressure Sensors (MOMPS) already showed much improved sensitivity and noise performance compared to their piezoelectric and capacitive counterparts, which makes them very promising for use in harsh environments, as e.g. for space applications or in biomedical fields where reliable and accurate sensors are required.
The goal of this project is to study the feasibility of other types of inertial sensor. The first step will be to investigate the performance of an optical accelerometer. Then if time allows, we will continue with the 3 axis gyroscope.



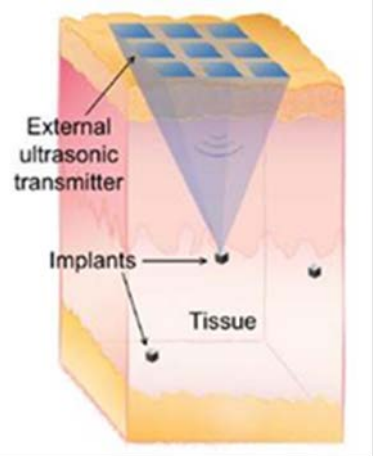
Type of project: Thesis project

Degree: Master in Science or Master in Engineering majoring in electrotechnics/electrical engineering, mechanical engineering, nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information for application, please contact Veronique Rochus (Veronique.Rochus@imec.be) and Roelof Jansen (Roelof.Jansen@imec.be).

Acoustic design for ultrasound power delivery for deep implant

We have seen an incredible transition in computing devices from vast compute servers that filled a whole room towards personal computers, laptops, tablets and smartphones. A similar revolution is happening in the medical diagnostic & therapeutic world. Recent years have seen a rapid rise of advanced (wearable) medical devices that bring high-quality medically-relevant diagnostics to an ever more convenient form factor at an even lower cost. More recently a shift is witnessed towards advanced implantable devices that can be implanted via minimally invasive procedures. Examples include ingestible, injectables, endoscopically implanted devices and subcutaneous implants. Imec is launching a major research effort into such advanced medical implant devices and we are looking for a good postdoctoral researcher to tackle a major hurdle in this field.
One of the biggest challenges to overcome in such highly miniaturized devices is the problem of power delivery. Most of the solutions today are battery-powered which has a number of severe limitations (toxicity, patient safety and size/volume). Hence there is a major interest to develop implants that can be wirelessly powered. In this area, inductively coupled devices are the most prevalent, but they rely on fairly large coils. RF-based wireless powering on the other hand is not efficient for deep implants due to the absorption of RF waves by human tissue. Ultra-sound however is a very interesting technique for medical implants and is already widely used for imaging. Ultra-sound is not absorbed as much by the human tissue, while ultrasound transducers can be made very small and even integrated into a chip.
In this master thesis, we will investigate an ultra-sound system for power delivery for extremely miniaturized deep implants. Based on acoustic simulations, we will first define the acoustic beam-forming technique and acoustic spec of the transducer to efficiently focus the energy to the implant. Then we will design the transducer for the optimal acoustic frequency. The work will be performed in collaboration with circuit designers working on the same topic.



Type of project: Thesis project

Degree: Master in Science or Master in Engineering majoring in electrotechnics/electrical engineering, mechanical engineering, nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information for application, please contact Veronique Rochus (Veronique.Rochus@imec.be), Nick Van Helleputte (Nick.VanHelleputte@imec.be) and Xavier Rottenberg (xavier.rottenberg@imec.be).

VII. Photovoltaics

PCB design, realization and characterization of local DC-DC convertor for smart configurable PV modules

It is well known that photovoltaic (PV) modules yield a lower energy in the field than what could be expected from their rated power, indicated as "Watt-peak (Wp)". The latter is measured under so-called "standard test conditions" but in climates like Western Europe, these are rarely met. In fact, the main energy yield losses (kWh/kWp) in these climates, can be attributed to a reduced illumination resulting in lower current, and non-uniform illumination conditions (shading, clouds, soiling, ...) leading to current mismatch in the serially connected cells inside the module. In order to maximize the power production of PV modules working under non-uniform illumination conditions, we are building advanced "smart" PV modules able to dynamically establish different non-series topologies. We want to build such configurable module demonstrators with specific topologies to test our research concepts, and to validate them by experimentally evaluating the Energy yield gain they allow for when working under non-uniform and dynamic irradiation and shading conditions. We also want to compare them with respect to standard state-of-the-art serially connected topologies. Currently, we are mainly interested in designing, prototyping and testing local DC/DC converters to finalize the first smart PV module demonstrator. The circuit design is innovative because voltages up to 10V input and 30V output, and current levels up to 15-20A have to be sustained while strongly minimizing cost and achieving acceptable losses and efficiency. And that is not achieved yet in commercial module and strong convertors. The MSc activity will firstly focus on PCB-level realization, characterization and testing of a switched-capacitors circuit concept which has already been simulated at imec. But now we want to build it in hardware. Later on, the MSc will also deal with the exploration of novel cost-effective inductor-based converter topologies. The entire project will have a clear impact on relevant aspects of the future photo-voltaic energy landscape. It combines mostly practical skills with a more in-depth analysis of the obtained results. The MSc activities will be co-guided with colleagues from the Ghent University and the MSc activities will mainly take place at their location. Considering the variety of challenges to be addressed, it is important for us to have a candidate who already has previous hands-on experience with electrical measurements and convertor characterization. A strong background in the domains of power electronics, preferably applied to photovoltaic sources, and control is desirable. However, given that we work on this with a team, the specific focus of the MSc subgoals within the topic can be adapted to some extent to the interest of the applicant.

Type of project: Thesis or internship project, or combination of both

Degree: Master in Engineering Technology or Master in Engineering majoring in electrotechnics/electrical engineering, energy

Responsible scientist(s):
For further information for application, please contact Patrizio Manganiello (Patrizio.Manganiello@imec.be), Francky Catthoor (Francky.Catthoor@imec.be) and Pieter Bauwens (pieter.bauwens@ugent.be).

Advanced thin film solar cell architectures

The field of photovoltaics (PV) is composed of thin film (TF) and silicon (Si) solar cells, where TF solar cells have a rather simple cell structure, while the typical Si solar cell design is more complex as it is optically and electrically optimized. Standard TF solar cell devices are grown layer by layer on a rigid or flexible substrate. For example for copper indium gallium (di)sulfide or (di)selenide (Cu(In,Ga)(S,Se)2 = CIGS(e)) solar cells: First a molybdenum (Mo) rear contact is deposited, then the
– typically 2.5 to 3.0 µm thick – CIGS(e) absorber layer, followed by a CdS buffer layer, and completed by an i-ZnO/ZnO:Al window layer. The typical Si solar cell design is more advanced, as it includes concepts to improve front and rear surface passivation, and optical confinement, as is the case for the passivated emitter and rear solar

cell (PERC). The main reasons to introduce these advanced technologies is to reduce charge carrier recombination at the front and rear Si surfaces (by means of front and rear surface passivation layers) and increase optical confinement (by means of front texturing and highly reflective rear surface passivation layers), and consequently enhance the efficiency of ever thinner Si solar cells.
You will be part of a team that aims to revolutionize the design of CIGS(e) TF solar cells by implementing advanced surface techniques, introducing structures and layers also used in Si solar technology. This includes adding innovative reflective rear contacts to capture more light into the cell's active layers. Other new techniques envisaged are inversion layer emitters, passivated contacts and surface passivation layers. In combination, these new techniques should lead to cells with enhanced conversion efficiencies, and improved stability and reliability.
This study of advanced TF solar cell architectures remains at the forefront of TF solar cell research, where physicists, engineers and chemists have the ability to successfully contribute. So, if you are interested in this work, then please contact the supervising scientist to find out if your profile fits this research.

Type of project: Thesis or internship project, or combination of both

Duration: 6 months

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in electrotechnics/electrical engineering, energy, materials engineering, chemistry/chemical engineering, nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information for application, please contact Bart Vermang (Bart.Vermang@imec.be).

Investigating the role of encapsulant adhesion on the reliability of a photovoltaic module

Photovoltaic (PV) modules, also known as solar modules are gaining in popularity and installed capacity. The technology is proven and deemed reliable and backed with a constant development of new technologies which could improve this further. However, it is very difficult to determine how reliable a new PV technology actually is. A phenomenon which is often occurring in PV modules after prolonged field exposure is delamination, which is driven by factors such as temperature, humidity, time and UV. When a module delaminates, the adhesion between the encapsulant (which protects the module against moisture ingress) and the glass, silicon or other interface deteriorates. At imec we have developed a new technique in measuring the adhesion. To acquire further insights on how these encapsulant-interfaces degrade, samples will have to be made to represent different substrates by using the newly developed methodology. These substrates will be exposed to different stress environments in an effort to establish relations between the types of stress, the adhesion strength as well as the types of encapsulant. Besides running multiple experiments, gaining a theoretical insight on how the adhesion manifests is also important. Some knowledge on material research is recommended and the work will take place at Energyville a new facility that occomodates a collaboration between imec and University of Hasselt. All necessary charactization and production tools are readitly available and a continuous supervision is provided by a PhD student.

Type of project: Internship project

Duration: 6 months

Location: Energyville, Genk (Belgium)

Degree: Master in Engineering Technology or Master in Science majoring in materials engineering

Responsible scientist(s):
For further information for application, please contact Philippe Nivelle (philippe.nivelle@imec.be), Eszter Vörösházi (eszter.voroshazi@imec.be) and Michael Daenen (michael.daenen@uhasselt.be).

Fabrication and optoelectronic characterization of high band gap thin film solar cells

Next to Si-based solar cells, devices based on chalcogenide thin films such as Cu(In,Ga)(S,Se)2 (CIGS) are at the forefront in thin film solar cell technology. Present Si and thin film photovoltaic (PV) technologies have already achieved power conversion efficiencies in excess of 20 %. In order to improve the conversion efficiencies beyond 30%, tandem solar cell technologies will be needed. CIGS based materials can be interesting high band gap materials for a tandem device structure as both Cu(In,Ga)S2 and CuGaSe2 have band gaps that exceed 1.5 eV and could be well integrated with Si bottom solar cells.
This master thesis topic consists of the fabrication and electrical and optical characterization of these high band gap chalcogenide absorber layers and solar cells.
The absorber layers will be fabricated using a two-step selenization approach consisting in evaporation of a metal layer stack followed by a selenization process at high temperatures. The fabricated layers will then be characterized using physical, electrical and optical measurement techniques.
Electrical measurements to be performed consist of current-voltage and capacitance-voltage measurements of thin film solar cell structures. All measurements will be performed as a function of temperature and illumination intensity, in order to fully characterize the diode parameters of the solar cell structure and to gain insight into the dominant recombination processes in the cell.
Optical measurements to be performed consist of temperature and intensity dependent photoluminescence and time-resolved photoluminescence measurements. These measurements will allow further insight into the different recombination mechanisms in the solar cells.
The different characterizations will be linked to the growth of the absorber in order to optimize the absorber quality for solar cell applications.

Type of project: Thesis or internship project, or combination of both

Duration: 6 months

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in materials engineering, energy, nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information for application, please contact Guy Brammertz (brammert@imec.be).

Characterization of poly-Si based passivated contacts

In the last years, PV manufacturing has seen a shift from Al-BSF (Back Surface Field) to PERC (Passivated Emitter and Rear Contact) solar cells to drive down the recombination current at the rear surface of the cells. Other shifts, e.g. transition from multicrystalline to monocrystalline material and from p-type to n-type base doping, are also taking place to minimize recombination currents in the bulk of the device. This evolution, combined with the advantages of using bifacial devices (energy contribution by rear illumination), is expected to lead to an increased market share of n-type bifacial PERT (Passivated Emitter and Rear Totally diffused) devices. The weakest point of these devices is the recombination at the interface between the silicon wafer and the metal contact. This problem can be mitigated using passivated contacts, shielding the minority carriers in the silicon wafer from the recombination centers at the metal contact while allowing fluent transport of the majority carriers to the same contacts. The focus of this Master Thesis will be on the characterization of poly-Si based passivated contacts for bifacial nPERT cells in combination with next-generation metallization techniques such as plating. The current research on this topic at imec focuses on optimizing the specs of the tunnel oxide in between the silicon bulk and the poly-Si layer, and the optimization of the poly-Si

layer itself (thickness, doping,...) to achieve a recombination current and a specific contact resistance as low as possible. This development aims at the implementation of the poly-Si layer at the backside of a bifacial solar cell, and will be followed by a feasibility study for integration at the front surface of these devices. The experimental work during this Master Thesis will be conducted on both monitor test structures and complete solar cell devices fabricated in equipment available in imec's state-of-the-art R&D solar cell line. The research will make use of advanced characterization tools (examples: photoluminescence, spectral response, current-voltage measurements,...) and material analysis techniques (examples: scanning electron microscopy, energy dispersive spectroscopy, x-ray diffraction) also available at imec.

Type of project: Internship or thesis project

Duration: 6 months

Degree: Master in Engineering majoring in energy, nanoscience/nanotechnology, electrotechnics/electrical engineering

Responsible scientist(s):
For further information for application, please contact Filip Duerinckx (Filip.Duerinckx@imec.be) and María Recamán Payo (Maria.RecamanPayo@imec.be).

Investigation on reversible degradation of perovskite solar cells under light-darkness cycling

In recent years, perovskite solar cells (PSCs) have been intensively studied. The certified power conversion efficiency of PSCs has exceeded 22%, which already caught up with commercially available thin film photovoltaics such as CdTe or CIGS. Despite high efficiency, commercialization of PSCs is hindered by stability issues. Under continuous illumination, PSCs often show an irreversible degradation. However, in real life solar cells naturally undergo light-darkness cycling over day–night periods. Some literatures have reported when PSCs go through such cycling the efficiency decays during illumination and recovers after storage in darkness, which is a unique feature for PSCs among all photovoltaics. It is of our interest to investigate how device architecture and cycling period influence this behaviour as well as the scientific explanation behind the reversible degradation. We are looking for a candidate who is motivated to join this frontier research. The work will involve hands-on fabrication of thin film PSCs, chemical/optical/electrical characterizations and data analysis. The candidate will benefit from the extensive knowledge and expertise of our team and work in a dynamic state-of-the-art research environment where physicists, chemists, and engineers collaborate efficiently.

Type of project: Internship or thesis project, or combination of both

Duration: 6 months

Location: Energyville, Genk (Belgium)

Degree: Master in Engineering Technology or Master in Science majoring in energy, nanoscience/nanotechnology, electrotechnics/electrical engineering, physics, materials engineering

Responsible scientist(s):
For further information for application, please contact Wenya Song (Wenya.Song@imec.be).

Defining optimal conditions for performance measurements of perovskite thin film PV modules

Perovskite thin film photovoltaic technology has shown remarkable improvements in performance in the past decade of research, with certified efficiencies comparable to commercially available 2nd generation photovoltaic technologies. Even though this exciting technology is suitable for many applications, further research and understanding of stability and upscaling of this technology are needed. Moreover, performance measurements of perovskite PV devices have shown to be non-trivial, depending on various measuring conditions. Thin-film PV group at Imec is one of the leading groups when it comes to research of upscalability of perovskite PV technology, with a goal to access its potential for eventual BIPV applications. In order to fairly access this potential we focus on defining optimal conditions for fair comparison of measured devices. Current research focuses on small lab devices, with aim to transfer the knowledge to larger area modules. The goal of this work is to analyze and define effects and conditions that affect perovskite module performance during laboratory testing, in order to fairly compare cell-module and module-module performance. Intern/student will have an opportunity to work in highly motivating environment with cutting-edge technology and state of the art laboratory settings. This experience will help gain an insight into this challenging new field and its opportunities.

Type of project: Internship or thesis project

Duration: 6 months

Location: Energyville, Genk (Belgium)

Degree: Master in Science or Master in Engineering majoring in energy, nanoscience/nanotechnology, electrotechnics/electrical engineering, physics

Responsible scientist(s):
For further information for application, please contact Lucija Rakocevic (Lucija.rakocevic@imec.be).

Understanding and overcoming instability in perovskite thin film PV modules

Perovskite based thin film PV technology has shown remarkable potential to become one of the next commercialized technologies. Perovskite based solar cells have seen improvements in power conversion efficiency that reach commercially available technologies after only a decade of research. As a thin film solution processed technology, perovskite based PV offers easily processed, low-cost, high-efficient technology needed for applications from BIPV to low power electronics. Nevertheless, for commercialization of perovskite PV technology further research into stability and upscalability of these devices is needed. Significant efforts are put into pushing the limits of knowledge when it comes to stability of perovskite solar cells. Thin film PV group at Imec focuses on researching intrinsic stability of perovskite solar cells, as well as upscaling perovskite cells into modules. During their time at Imec, student will focus on understanding and overcoming the instabilities of perovskite modules in comparison to small area cells when exposed to mono-stress stability testing. The student will have an opportunity to work with cutting-edge technology in state of the art labs. Through collaboration with Imec colleagues they will gain insight into specifics of this exciting new PV technology.

Type of project: Internship or thesis project

Duration: 6 months

Location: Energyville, Genk (Belgium)

Degree: Master in Science or Master in Engineering majoring in energy, nanoscience/nanotechnology, electrotechnics/electrical engineering, physics, materials engineering

Responsible scientist(s):
For further information for application, please contact Lucija Rakocevic (Lucija.rakocevic@imec.be) and Wenya Song (Wenya.song@imec.be).

Performance optimization of bifacial photovoltaic systems

Photovoltaic (PV) solar panels provide a very attractive solution for future clean energy. However, the deployment of PV systems is strongly driven by the levelized cost of electricity (LCOE). Therefore, imec is developing PV modules with additional or novel components and/or novel cell technologies to improve the energy yield and thereby reducing the LCOE. Recently, bi-facial PV modules gained enormous attenuation as these devices are able to collect light from both the front and the rear side. As a result, the PV modules can also convert (ground) reflected light into electrical energy. The reported power gain varies between 5–30%. However, the energy production gain during outdoor conditions depends on a large number of parameters e.g. climate conditions, surface reflection, row spacing, etc. Next to that, ground reflection creates a non-uniform illumination on the rear of the module, and as solar cells are connected in series, the energy yield of bifacial modules is affected by mismatch losses. To estimate the energy yield of bi-facial modules, and to evaluate the mismatch losses and potential solutions, more insight into the outdoor performance of these novel modules is required. The present project focuses on optimizing the outdoor performance of bifacial PV modules by means of interdisciplinary computer simulations performed using the Energy Yield modelling framework developed at imec.
The candidate will model outdoor PV installations under real climatic conditions in order to find the configuration leading to maximum bifacial light collection. The candidate will also evaluate the energy yield of the best configurations by simulating optical, thermal and electrical mechanisms taking place within the PV modules during the energy conversion process. Working on this subject will allow the candidate to strengthen his/her skills in programming in Matlab, Python and Shell; high performance computing; thermal, electrical and optical modelling, data processing and visualization. The results of the study will contribute to the development of a rising PV technology, which will undoubtedly play an important role in the green energy transition.

Type of project: Internship project

Duration: 6 months

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in energy, physics, computer science

Responsible scientist(s):
For further information for application, please contact Imre Horvath (imre.t.horvath@imec.be), Hans Goverde (hans.goverde@imec.be) and Eszter Voroshazi (Eszter.Voroshazi@imec.be).

VIII. GaN Power Electronics

There are currently no Master thesis/internship projects available in this research domain.

IX. Wireless IoT Communication

Low-power ADC for radar sensing

The demand for inexpensive and ubiquitous accurate motion-detection sensors for road safety, smart homes and robotics justifies the interest in single-chip mm-Wave radars: a high carrier frequency allows for a high angular resolution in a compact multi-antenna system and a wide bandwidth allows for a high depth resolution. With the objective of single-chip radar systems, CMOS is the natural candidate to replace SiGe as a leading technology. Radar solutions in advanced CMOS technology offer a path to lower power, more compactness, higher levels of integration, and low cost. These will allow the use of low-power, battery-operated radar systems in many new application domains in the upcoming Internet-of-Things (IoT) society.
Radar systems often suffer from high spillover (i.e. signal leaking from the transmitter to the receiver) levels, which increase the required dynamic range of the receive chain. Besides the use of several mitigation techniques in the mmwave section of the receiver, an equally important building block is the high-resolution analog-to-digital converter (ADC) that digitizes the reflected signal before signal processing in the digital signal processor. Performance requirements are a resolution of >12 bits and sampling speed up to 100MS/s, to be obtained with power consumption in the mW level.
Imec's IoT research group has a long-standing track record in the design of power-efficient RF and mmwave transceivers and ADCs, and is looking for a motivated Ms student to investigate the design of such and ADC. Knowledge of analog design basics, and Cadence/specter tools is a must. The research project will consist of a literature study, architecture investigations and trade-offs, followed by details circuit design and simulations. Depending on progress, layout and/or tapeout and measurements is also possible.

Type of project: Thesis with internship project

Degree: Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information for application, please contact Jan Craninckx (jan.craninckx@imec.be) and Piet Wambacq (piet.wambacq@imec.be).

Wideband mm-wave front-end circuits for 5G applications

For next generation 5G wireless communications, millimeter wave frequencies are utilized as carrier frequencies due to the availability of large bandwidths. This promises a large capacity leading to higher throughputs. Advanced technology nodes are now capable of enabling radio transceivers operating at mm-wave frequencies.
Front end circuits include components such as power amplifiers (PA's), low-noise amplifiers (LNA's), variable-gain amplifiers (VGA's) and phase shifters. To achieve long-range communication distances, a cascade of several of these blocks is usually required. This limits the possible overall circuit bandwidth, reducing the number of available communication channels in the system.
In this research project, techniques to improve the circuit bandwidth of a transmit front-end will be explored at 28 GHz and validated at both schematic and layout levels. The successful candidate will start first by a literature review, analyzing bandwidth improvement techniques for both the active and passive components, and finally applying them to the front-end.

Type of project: Thesis with internship project

Duration: 6 months

Degree: Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information for application, please contact Jan Craninckx (jan.craninckx@imec.be) and Piet Wambacq (piet.wambacq@imec.be).

Smart radars: machine learning for radar signals

Thanks to the constant evolution of semiconductor technology, millimeter-wave radars can now be implemented in a single chip including the transmitter, receiver and DSP. This highly integrated implementation makes consumer grade radar applications possible such as automotive radar, indoor or outdoor surveillance, gesture recognition and vital sign monitoring. Imec has developed several high-resolution CMOS radar chips. These chips are connected to a digital platform for further processing, demonstration and application development.
The goal of this thesis is to further extend the platform functionality and experiment with the imec radar (and possibly other radars) in various environments targeting different applications. It is expected that the student uses potentially a broad range of machine learning techniques, from hand crafted feature extraction to fully supervised deep learning to analyze radar data to solve application-dependent classification problems. This work will be performed with a team working on all aspects of the radar, from RF to software.
The candidate must show a good understanding of graduate level signal processing theory, proficiency in programming using Matlab, Python and C/C++. It is desirable to have a good hold on statistical learning, pattern matching and state of the art AI techniques. Some knowledge of radar concepts is a plus.

Type of project: Thesis with internship project

Duration: 6 months thesis and optional 3 months internship

Degree: Master in Engineering majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information for application, please contact Karthick Parashar (Karthick.Parashar@imec.be) and André Bourdoux (Andre.Bourdoux@imec.be).

X. Solid State Batteries

Development and synthesis of dual electron and ion conductive materials for advanced Li-ion batteries

The Li-ion cell is the technology of choice for rechargeable battery applications as Li-ion insertion electrodes provide the highest volumetric and gravimetric energy density known. The Li-ion electrode formulation currently consists of: (1) active electrode powder material, (2) carbon as electronically conductive additive, (3) polymer binder and (4) Li-ion electrolyte. Essential for good operation is good electrical contact between the active electrode particles and the carbon which provides current collection through the composite layer as well as good contact between the electrode and the electrolyte, which will shuttle the Li-ions between the two battery electrodes.
Innovations in the electrode architecture are necessary to maximize the fraction of the active storage material in the electrodes without penalty in kinetic performance. This project contributes to the innovation in the electrode architecture through the study and development of dual ionic and electronic (i/e) conductor materials with enhanced ionic and electronic conductivity. The overall objective of this project is the study and development of dual ionic-electronic conductor coatings, with the purpose of enhancement of the Li-ion cell performance towards maximized accessible capacity and energy density, charging rate and life time.
In the master thesis, a method to synthesize novel dual electronic and ionic conducting materials will be developed. The electronic and ionic conductive properties of the materials will be characterized through a combination of cyclic voltammetry, impedance spectroscopy and DC transient measurements on thin-film model systems. The electrochemical measurements will be complemented by an extensive physical characterization (ERD, XRD, EDX, RBS,...) of the newly developed materials.

Type of project: Thesis project

Degree: Master in Science or Master in Engineering majoring in chemistry/chemical engineering, materials engineering, nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information for application, please contact Louis DeTaeye (Louis.Detaeye@imec.be).

Heterogeneous conductivity enhancement in solid state electrolytes for all-solid-state lithium ion batteries

Lithium-ion batteries (LIBs) with a solid-state electrolyte can potentially solve two key limitations of today's LIBs with liquid electrolytes, namely, safety issues due to the flammability of the electrolyte solution and cycle life time issues due to unwanted side-reactions at the solid/liquid interface. The improved safety and potentially extended lifetime of solid-state LIBs makes them highly desired, however, finding a solid-state electrolyte with Li+ conductivity comparable to the existing liquid electrolytes (1-10 mS/cm) that also exhibits good electrochemical stability turns out to be extremely challenging. Utilizing heterogeneous doping in composite electrolytes is one promising concept for solving these challenges. Heterogeneous doping refers to the significantly enhanced ion transport that occurs at the interface between an oxide insulator and a Li-ion conductor. Through combinations of oxides, surface functionalization and Li-ion conductors the conductivity of the interface region can be further optimized.
This thesis project focuses on gaining fundamental insights in the interface conductivity between oxides and Li-ion conductors. The interface conductivity will be benchmarked to bulk conductivities using a thin-film platform with emphasis on interface control and functionalization, both through gas-phase deposition and sputter deposition. Controlled deposition of thin film electrolyte layers using sputter deposition or atomic layer deposition will be a big part of the project. Next to the process optimization and physical characterization, large effort will go into the electrical and electrochemical characterization of the bulk electrolyte and the interface region. The experimental work of the project is carried out at imec facilities. Next to the fully equipped battery lab and thin-film deposition

facilities, the imec state-of-the-art nanofabrication and characterization facilities will be available to carry out the research.

Type of project: Thesis project

Degree: Master in Science or Master in Engineering majoring in bioscience engineering, chemistry/chemical engineering, materials engineering, nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information for application, please contact Simon Hollevoet (Simon.Hollevoet@imec.be).

Lithium alloys as reliable anode materials for Li-ion batteries

By 2025, 25% of the cars sold worldwide are projected to be an electrical car. Growing awareness by governments and customers that electrical cars in conjunction with renewable energy can improve local living conditions and the conviction that this technology could shake up automobile industry are fueling the ongoing rise of battery research. Thanks to its high capacity (Ah/L), Li-ion batteries currently shape the main development route. In this technology, where a Li-ion is exchanged between cathode and anode, the typical anode material is carbon or Li4T5O12. Employing Li metal as anode would drastically increase both the capacity and the output potential of the battery cell, but is inhibited by parasitic reactions at the Li surface limiting cell performance. Moreover, large Li dendrites grow on the anode during cycling, ultimately leading to dangerous shorting of the cell. Striking possible alternatives are Li-alloys such as Li-Al or Li-In. Indications are that Li-alloys can bypass these mentioned issues while maintaining high capacity and cell voltage.
During this master thesis, we will study the electrochemical behavior of Li-alloys as function of composition. Different alloys (Al, In...) and different techniques to fabricate them (evaporation, plating, dry milling and pressing...) will be compared. The stability of the alloy in combination with appropriate electrolytes will be determined by standard electrochemical measurements. Focus will be on the interaction with imec's solid electrolytes, another key enabler to obtain safe and high capacity batteries. Charge and discharge behavior and cycling performance will be evaluated in battery cell. Possible dendritic growth will be visualized by Scanning Electron Microscopy. Final goal of the thesis is to deliver an anode that can serve in the process of reference for solid-state batteries at imec.

Type of project: Thesis project

Degree: Master in Science or Master in Engineering majoring in bioscience engineering, chemistry/chemical engineering, materials engineering, nanoscience/nanotechnology, energy

Responsible scientist(s):
For further information for application, please contact Maarten Debucquoy (Maarten.Debucquoy@imec.be).

Modelling of a solid-composite electrolyte for Li-ion batteries

Lithium-ion batteries (LIB) with a solid-state electrolyte can potentially solve two key limitations of today's LIB with liquid electrolytes, namely safety issues due to the flammability of the electrolyte and cycle life time problems due to unwanted side-reactions at the solid/liquid interface. The improved safety and potentially extended lifetime of solid-state LIB makes them highly desired. However, finding a solid-state electrolyte with a Li-ion conductivity comparable to existing liquid electrolyte solutions (~10 mS/cm) that also exhibit good electrochemical stability turns out to be extremely challenging.
The energy storage team in imec recently developed a solid-state composite electrolyte (SCE) with a Li+-ion conductivity exceeding 1 mS/cm. In composite electrolytes, the lithium-ion conductivity is enhanced by so-called heterogeneous doping i.e. an enhanced ion conductivity at the interface between an oxide and a lithium salt. The

composite electrolyte developed at imec is a monolith composed of a nanoporous oxide matrix (SiO2) filled with an Li-ion electrolyte. Conductivity enhancement in two-phase composite systems has been known for almost 90 years. However, the fundamental mechanism of the phenomenon is still poorly understood. Atomistic modelling techniques are powerful tools that provide predictive insights on an atomic scale on the factors that determine the composite electrolyte conductivity. In this master thesis project, computational methods will be used to help unravel the nature of the conductivity enhancement.

Type of project: Thesis project

Degree: Master in Science or Master in Engineering majoring in chemistry/chemical engineering, materials engineering, nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information for application, please contact Eva Van Daele (Eva.Vandaele@imec.be) and Maarten Mees (Maarten.Mees@imec.be).

XI. Data Science and Data Security

There are currently no Master thesis/internship projects available in this research domain.

XII. Process and Hardware Engineering

Automation of atomic force microscopy measurements

Atomic Force Microscopy (AFM) is a heavily used technique at imec to assess the nano-scale topological and electrical properties of surfaces with an extremely sharp probe. Information on properties such as surface roughness, dimensions of nanoscale features, atomic terraces, grain boundaries, conductivity, work function and many more provide important feedback for newly developed materials and processes. To cope with the increasing demand we have recently installed new software enabling us to automatically measure a number of samples via a sort of recipe. The ultimate goal of this internship will be to automate the entire AFM measurement, the data analysis and the report creation in order to significantly improve the output of the AFM tool. To achieve this, the student is expected 1) to create and write recipes with the software, and explore its capabilities, 2) to investigate and optimize the measurement conditions (various probes, various modes), 3) to automate the data analysis/reporting via the existing software or self-developed software (for instance in Matlab). The ideal student thus has: an interest/background in automation with an affinity for software and nanophysics, a can do attitude and the ability to work independently. We offer a project that (if successful) will have a major impact on our operational results, thorough training on the tool and existing software and an ambitious team to work in.

Type of project: Internship project

Duration: 6 months

Degree: Master in Engineering Technology majoring in electrotechnics/electrical engineering, computer science, materials engineering, nanoscience/nanotechnology, physics

Responsible scientist(s):
For further information for application, please contact Kristof Paredis (Kristof.paredis@imec.be) and Danielle Vanhaeren (Danielle.Vanhaeren@imec.be).

Structural implementation of defectivity for QC

In conventional far back-end of line of Integrated Circuits (IC) manufacturing, wafers are singulated into individual IC's and then assembled in a plastic/epoxy package with leads or solder bumps to connect to the Printed Circuit Board (PCB). The consumer and high performance device markets are imposing more challenging requirements on footprint, number of I/O connects, speed, energy efficiency, etc. To meet these requirements, packaging IC's is shifted more earlier in the manufacturing process, namely on wafer level instead of individual IC's, i.e. Wafer-Level Packaging (WLP). Device connections are then processed on wafer level using wafer fab processes. As a result, connections can be made smaller (scaling) which is beneficial for I/O density on same chip footprint, speed and bandwidth of the device.
There is no single standard in industry for WLP and mutliple flavours exist. At imec, multiple WLP techniques are explored. One of that is Fan-Out WLP (FOWLP). It is an enhancement of standard WLP for a greater number of I/Os and system-in-package (SiP) solutions. FOWLP involves dicing IC's on silicon wafers (logic, memory, etc) and then very precisely positioning the known-good dies on a carrier wafer, which is then molded, following by making redistribution layers (RDL) on top of the molded area and then forming bumps to connect to the outside world of PCB for example.
RDL also need to be scaled and from industry there is a roadmap towards 2um line/space and below. At imec we are developing a fine-pitch RDL (FPRDL) process. Random defects are still present, meaning multiple defect types across the full wafer. An inventory of these defect types need to be made and root causes need to be identified in order to improve the process. When improvements are implemented, failure mechanisms in the process are understood and no random defects are present with acceptable yield, the process is mature and process control can be establised.

The topic of this thesis/internship is to contribute in bringing FPRDL to maturity. Defectivity and metrology will be used to characterize the process flow of making FPRDL. Inspection tools will inspect wafers for defects (automated inspections that captures defects in dies). These tools need to be trained to detect defects and intelligence need to be built in to classify these defects in different defect types. All this defect data need to be analysed by a Yield Management Software available at imec which enables creating defectivity plots and charts. Also measurements need to be done on metrology tools to verify critical dimensions (2D and 3D) of FPRDL.
Multiple wafers will be processed throughout the year to improve the process and validate/monitor maturity. This will ensure availability of sufficient data. The student will be able to understand the full process flow of FPRDL (CVD, lithography, electroplating, resist strip, etch, clean) and the impact of changing process parameters on the result. The student will also be trained to setup inspection recipes on inspection and metrology tools and to use the Yield Management Software to analyse the data and derive defectivity conclusions. One person from process engineering (metrology team) and one person from integration (research engineer that designed the process flow of FPRDL) will be available to coach the student regularly.

Type of project: Internship or thesis project

Degree: Master in Engineering Technology majoring in electrotechnics/electrical engineering, computer science, materials engineering, nanoscience/nanotechnology, physics, chemistry/chemical engineering

Responsible scientist(s):
For further information for application, please contact Maarten Liebens (Maarten.Liebens@imec.be) and John Slabbekoorn (jslabbe@imec.be).

XIII. Software Engineering

There are currently no Master thesis/internship projects available in this research domain.

XIV. Neuroelectronic Research (NERF)

Introduction

Imec, VIB (Flanders' leading life science institute), and the Leuven University have set up a joint basic research initiative to unravel the neuronal circuitry of the human brain: Neuroelectronics Research Flanders (NERF). Supported by the Flemish Government, NERF looks into fundamental neuroscientific questions through collaborative, interdisciplinary research combining nanoelectronics with neurobiology. It intends to push the boundaries of science, by zooming in on the working of neurons at an unprecedented level of detail. In the long run, NERF will generate new insights in the functional mapping of the brain, as well as research methodologies and technologies for medical applications, i.e. diagnostics and treatment of disorders of the central and peripheral nervous system. The NERF labs are located at the imec premises. Read more: http://www.nerf.be/.

Unraveling neuronal activity during locomotion

Plasticity in sensorimotor circuits is the basis of motor learning during development and after central nervous system trauma. Spinal cord injury disintegrates functional sensorimotor ensembles by disconnecting circuits below lesion from the rest of the nervous system. While an incomplete lesion is often associated with partial functional recovery, our lack of knowledge of the genetic identity, precise anatomical connectivity, and function of the participating circuit components poses a great challenge to understand and intervene in the process of motor recovery. Using flexible electrode technology available at imec, the aim of the project is to reveal neuronal activity of non-injured and injured spinal cord circuits **in real-time** during walking in a neuronal population specific manner in an unprecedented resolution. In this project we will use combined methods of mouse genetic engineering and viral technologies to identify neuronal populations involved in a given locomotor task with phase-specific temporal precision. Interns/students' responsibilities will include implementation of surgical technique for stimulation/recording electrodes, behavioral training, kinematic recording and analyses as well as bridging between collaborating technology teams and the Takeoka lab's neuroscience circuit expertise.

Type of project: Internship project

Duration: 6 months

Degree: Master majoring in bioscience engineering, electrotechnics/electrical engineering, nanoscience & nanotechnology, materials engineering

Responsible scientist(s):
For further information or for application, please contact Aya Takeoka (Aya.takeoka@nerf.be).

Using machine learning and deep neural networks to automatically identify components of neural circuits in the visual system

The shape and position of a neuron conveys critical information about its identity and function. The identification of cell types from structure is a classic method that relies on the time-consuming and labour intensive tracing of its structure. Recent advances in experimental and imaging techniques now allow the acquiring of data sets approation for data-driven approaches to neuronal circuit analysis feasible, with the caveat automated image processing pipelines become a necessity. Recent advances in deep neural networks and machine learning techniques have demonstrated

the power of these techniques to reliably perform automated image recognition and segmentation online. This work has begun to be translated to work in laboratory environments. The goal of this thesis/internship is to apply/develop these techniques to a set of imaging data where we would like to automatically identify to neuronal components involved in the processing of visual information. The suitable student should already be familiar with machine learning and imaging processing techniques, as well as have good knowledge of at least one programming language (preferably Julia, Python, MATLAB or C++).

Type of project: Thesis or internship project, or combination of both

Duration: 6 months

Degree: Master in Science or Master in Engineering majoring in bioscience engineering, electrotechnics/electrical engineering, computer science, physics

Responsible scientist(s):
For further information or for application, please contact Karl Farrow (karl.farrow@nerf.be).

Using virtual reality to study the function and neural circuits in the mouse visual system

The main aim of the lab is to understand the fundamental principles underlying the function of neural circuits during behavior. Towards this goal we investigate how sensory information is processed along the neural pathways that generate visually guided behavior. The lab uses two-photon calcium imaging, high-density probe recordings, optogenetics and computer based analytical methods of neural activity in awake behaving animals. Using these techniques, we study the activity of genetically defined neural populations in response to visual stimulation and perturb components of these circuits to understand their function in visual processing and visually guided behavior. Ultimately, the experiments are designed to understand the fundamental principles of sensory information processing in the brain. The visiting students are expected to have a decent background in computer programming, instrumentation and an interest in video game development. Together With the visiting student we will aim to build and use a virtual reality system that will allow us to record neural activity while the animal performs visually guided tasks, i.e. plays a video game. These experiments will allow us to investigate the processing of visual information with and without sensory feedback.

Type of project: Thesis or combination of internship with thesis

Degree: Master in Science or Master in Engineering majoring in bioscience engineering, electrotechnics/electrical engineering, computer science, physics

Responsible scientist(s):
For further information or for application, please contact Karl Farrow (karl.farrow@nerf.be).

Understanding memory through real-time processing and closed-loop manipulation of brain activity

The human brain is the most complex biological machine with over 80 billion active cells and a thousand times more interconnections between the cells. The Kloosterman laboratory at Neuro-Electronics Research Flanders (NERF, www.nerf.be) is interested in understanding how the brain learns about the world and how it uses this information for future benefit. For this, we probe the brain's memory system using large-scale measurements of electrical activity during the acquisition of memory tasks and subsequent sleep. These measurements provide a rich view on patterns of brain activity that mediate remembering, planning and decision making. We apply advanced data analysis

approaches to interpret the relation between brain activity and behaviour. To further reveal the causal role of specific activity patterns in cognition, we have developed novel algorithms and a custom software platform for real-time signal processing and closed-loop perturbations.
We are looking for highly motivated candidates who would like to advance our understanding of brain function in an international, multi-disciplinary and stimulating research environment. The candidates will work on the development of software tools for real-time processing of streaming experimental data and/or offline analysis of complex data sets. Candidates should have demonstrated programming experience (C++ and/or Python) and be familiar with digital signal processing, machine learning and/or neuro-statistics. The work will take place at the NERF laboratories on the imec campus. The candidates are expected to work pro-actively and independently within a small team of dedicated neuroscientists.

Type of project: Thesis or internship project, or combination of both

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in electrotechnics/electrical engineering, computer science, physics

Responsible scientist(s):
For further information or for application, please contact Fabian Kloosterman (fabian.kloosterman@nerf.be).

Engineering new devices and tools to study how the brain processes and stores information

Advancing our understanding of how the brain performs computations and supports cognition, requires sophisticated tools and devices for experimental read-out and manipulation of neural activity. In the Kloosterman laboratory at the Neuro-Electronics Research Flanders (NERF, www.nerf.be), we are interested in revealing the mechanistic principles of information processing and storage in the brain's memory system. For this, we develop and apply advanced brain implants and other tools for experimental neuroscience that enable large-scale monitoring of neural activity in animals that perform complex behavioural tasks. Examples include flexible neural probes integrated in 3D-printed arrays, implantable mini-microscopes and devices for automated behavioural control.
We are looking for highly motivated candidates with a background in Electrical Engineering, Mechanical Engineering or similar background, who would like to contribute to the design, fabrication and testing of new tools that advance experimental neuroscience. Candidates will work in the NERF laboratories on the imec campus, in an international, multi-disciplinary and stimulating research environment. Candidates need to be familiar with one or more of: electronics design, 3D CAD design, robotics & micro-controller platforms and programming (C++/Python). The ideal candidate is able to work pro-actively and independently in a small team of dedicated neuroscientists. For more information, please contact Prof. Fabian Kloosterman (fabian.kloosterman@nerf.be).

Type of project: Thesis or internship project, or combination of both

Degree: Master in Engineering Technology or Master in Science or Master in Engineering majoring in electrotechnics/electrical engineering, computer science, physics, mechanical engineering, nanoscience/nanotechnology

Responsible scientist(s):
For further information or for application, please contact Fabian Kloosterman (fabian.kloosterman@nerf.be).

XV. Microelectronics Design

Development of RadHard SAR ADC in 65nm CMOS

The purpose of this work is to design and layout a 12 bits 10 Msps SAR ADC. This design will be a part of the DARE65 library currently developed by IMEC IC-Link. The DARE65 platform (65nm technology) is developed in collaboration with the European Space Agency (ESA) and is the natural continuation of the DARE180 library developed during the past 15 years at IMEC.
Becasue the DARE65 platform is dedicated to space applications, all parts must be hardened against cosmic rays (neutron, proton, heavy ions...) existing outside the earth's atmosphere.
The cosmic rays have mainly 2 effects on the CMOS circuit:

- TID: the Total Ionization Dose result in an accumulation of charge trapped in the Silicon oxide interface. These charges may induce leakage between devices and/or may shift the transistor threshold and/or increase the device leakage.
- SEE: the Single Event Effects are due heavy ions passing through the silicon die and deposing electrical charge in the PN junction (from few tens of fC till few pC). This charge deposit can result in a latch-up and/or in a single-event transient and/or in a gate rupture...

The student can rely on in-house design knowledge: IMEC IC-Link has developed over the years specific tools and a design flow to harden designs for space applications:

- layout specific rules
- heavy ion electrical model
- automated heavy ions check
- edgeless transistor layout and simulation model

In order to go through the whole specification to layout flow, state of the art software is used. This requires the student to be present at imec on a regular basis. A basic, but solid understanding of analog design is required to implement the transistor level circuits. Prior software knowledge is not required.
Software used:

- Cadence Virtuoso (schema & layout), Analog Design Environment XL & Spectre (simulation)
- Mentor Calibre (layout verification)
- Linux OS

Type of project: Thesis or internship project

Type of study: 20% studying literature, 50% design & simulation, 30% layout

Duration: 6 months

Degree: Master in Science majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Laurent Berti (Laurent.Berti.ext@imec.be), Geert Thys (Geert.Thys@imec.be) and Jan Wouters (Jan.Wouters@imec.be).

Enhancements for RadHard IP in 180nm and 65nm CMOS

The purpose of this work is the design and layout of a Low-Voltage Differential-Signaling (LVDS) transmitter (TX) and receiver (RX) together with a Power-On-Control (POC) central unit. The role of the POC is to avoid any transient effects during the power ramp-up/down of the circuit (like huge transient current, transient glitch on I/O

pad, ..). All analog circuit designs must be done respecting RadHard design constraints for earth orbits and deep space missions e.g. galactic cosmic rays.
For more than 15 years imec IC-link develops, in cooperation with the European Space Agency (ESA), a radiation tolerant digital standard cell library and full custom IP (like band-gap, ADC, DAC, ..), in 180 nm CMOS. Currently IC-link is starting the development, again in cooperation with ESA, of a new radiation-tolerant library on a 65nm platform. The building blocks developed in this library will be mainly used in IC's dedicated to space application.
Because of the high energetic radiation existing outside the earth's atmosphere, all the elements of this library must be designed with specific techniques to protect the circuit against radiation effects (e.g. gamma ray) and against heavy ion strikes. A heavy ion striking a PN junction will inject a charge of few tens of fC till few pC. The art/challenge of the radiation hardened design is to be insensitive/immune to this important charge deposit.
LVDS is an electrical standard for high speed digital communication at system level. The electronics implementing this standard are essentially analog. On top of the LVDS standard, we require for these IPs cold-spare capability for the LVDS RX and TX and fail-safe capability for the LVDS RX.

- Cold-spare: possibility to put several chips in parallel, with only one powered. The other chips are grounded. In case of error, defect on the powered chip, we can easily power another chip to replace it.
- Fail-safe: this functionality will detect the presence or not of signal on the LVDS line.

In order to go through the whole specification to layout flow, state of the art software is used. This requires the student to be present at imec on a regular basis. A basic, but solid understanding of analog design is required to implement the transistor level circuits. Prior software experience is not required.
Software used:

- Cadence Virtuoso (schematic & layout), Analog Design Environment XL & Spectre (simulation)
- Mentor Calibre (layout verification)
- Linux OS

Type of project: Thesis or internship project

Type of study: 15% studying literature, 50% design & simulation, 35% layout

Duration: 6 months

Degree: Master in Science majoring in electrotechnics/electrical engineering

Responsible scientist(s):
For further information or for application, please contact Giancarlo Franciscato (Giancarlo.Franciscato@imec.be), Geert Thys (Geert.Thys@imec.be) and Jan Wouters (Jan.Wouters@imec.be).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