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3D system integration

# A design-for-test standard for test access in 3D integrated circuits

**Recently, a new standard for die-level design-for-test (DfT) features in 3D integrated circuits (3D ICs) was published by IEEE Standards Association. The standard, called IEEE Std 1838™-2019, describes how to build a test access architecture that makes it possible to test individual dies once they are stacked to form a 3D IC. In other words, it allows stacked dies in 3D ICs to cooperate such that all of them can connect with external test equipment. The standard is available through the IEEE Xplore Digital Library.**

In the online media resource 3D InCites, Erik Jan Marinissen, scientific director at imec and founder and first chair of the IEEE standardization working group on 3D-DfT, talks about the standardization effort, and discusses the standard itself and its importance for the 3D-IC community.

Read part 1 and part 2 of the full article in 3D InCites.

## Want to know more?

- The 3D designfor-test standard (IEEE Std 1838TM2019) was published on the website of the IEEE Standards Association. A copy can be purchased here.
- If your company or university subscribes to IEEE Explorer, you may have free access here.
- Read imec's press release on the standardization of 3D DfT.