Intro

Interconnects, the tiny wiring schemes in chips’ back-end-of-line (BEOL), are becoming more compact at each technology node. This, in turn, is causing an undesired increase in the resistance-capacitance (RC) delay in chips. Researchers worldwide are therefore developing new strategies to enable effective interconnects for the next generations of chips.

Zsolt Tokei, imec’s Director of the Nano-Interconnect Program, discusses the new trends in the BEOL landscape. He presents some of imec’s alternative process options, materials and design solutions that promise to overcome the RC delay challenge.
The proposed solutions have been presented at the 2017 IEEE International Interconnect Technology Conference (IITC), where Zsolt took part in a panel discussion on the most promising next-generation metal interconnecting wires.

**RC delay, a concern for the IC industry**

With the 7nm technology node in the development phase and the 5nm node moving into development, transistor scaling gets ever more complex. On top of that, the performance benefits gained at the front-end-of-line (i.e., the transistors) can easily be undone if the back-end-of-line can’t come along. BEOL processing involves the creation of stacked layers of Cu wires that electrically interconnect the transistors in the chip. Zsolt Tokei: “Today, high-end logic chips easily have 12 to 15 levels of Cu wires. With each technology node, this Cu wiring scheme becomes more complex, mainly because there are more transistors to connect with an ever tighter pitch. Shrinking dimensions also means the wires have a reduced cross-sectional area, which drives up the resistance-capacitance product (RC) of the interconnect system. And this results in strongly increasing signal delay.”

“The RC delay issues started a few nodes ago, and the problems are becoming worse. For example, a delay of more than 30% is expected when moving from the 10nm to the 7nm node.”

**The current BEOL flow**

Cu-based dual damascene has been the workhorse process flow for interconnects since its introduction in the mid 1990s. A simple dual damascene flow starts with the deposition of a low-k dielectric material on a structure. These low-k films are designed to reduce the capacitance and the delay in the ICs. In a next step, this dielectric layer is covered with an oxide and a resist, and vias and trenches are formed using lithography and etch steps. These vias connect one metal layer with the layer above or below. Then, a metallic barrier layer is added to prevent Cu atoms from migrating into the low-k materials. The barrier layers are deposited with physical vapor deposition, using materials such as tantalum and tantalum nitride, and subsequently coated by a Cu seed barrier. In a final step, this structure is electroplated by Cu in a chemical mechanical polishing (CMP) step.

**A 5nm technology full dual damascene module**

The semiconductor industry is hugely in favor of extending the current dual damascene technology as long as possible before moving to a new process. And this starts with incremental changes to the current technology, which should suffice for further scaling to at least the 5nm technology node.
“At this node, the BEOL process becomes extremely complex, and interconnects are designed at very tight pitches. For example, a 50% area scaling in logic and 60% scaling of an SRAM cell from 7nm to 5nm results in a gate pitch at around 42nm and an intermediate first routing metal at 32nm pitch (or 16nm half pitch, which is half the distance between identical features). In these BEOL layers, trenches are created which are then filled with metal in a final metallization step. In order to create electrically functional lines, perpendicular block layers to the trenches are added, where metal traces are not formed. One of the many challenges to scaling the interconnects relates to the patterning options. Patterning these tight pitch layers is no longer possible by using single immersion lithography and direct etch steps. Only multi-patterning – which is known to be very costly and complex – is possible either by immersion or by EUV or by a combination of immersion and EUV exposures to form a single metal layer. At IITC, we showed a full integration flow using multi-patterning, which enables us to pattern tight-pitch metal-cut (the blocks), and effectively scale the trench critical dimension to 12nm at 16nm half pitch. We also looked at the reliability, for example at electromigration issues caused by the movement of atoms in the interconnect wires. We demonstrated the ability of our Cu metallization scheme at 16nm critical dimension with extendibility to 12nm width, and investigated full ruthenium (Ru) metallization as copper replacement.”

Tight pitch copper lines embedded into a low-k material. The metal cuts (or blocks) were enabled by a tone-inversion flow.
Scaling the BEOL beyond the 5nm node...

For the technology nodes below the 5nm, the team of Zsolt Tokei is investigating a plethora of options and comparing their merits. Options include new materials for conductors and dielectrics, barrier layers, vias, and new ways to deposit them; innovative BEOL architectures for making 2.5D/3D structures; new patterning schemes; co-optimization of system and technology, etc.

Zsolt Tokei: “For example, to achieve manufacturable processes and at the same time control the RC delay, we increasingly make use of scaling boosters, such as fully self-aligned vias. Via alignment is a critical step in the BEOL process, as it defines the contact area between subsequent interconnect levels. Any misalignment impacts both resistance and reliability. We have shown the necessity of using a fully self-aligned via to achieve overlay specifications, and proposed a process flow for 12nm half pitch structures.”

Also, self-assembled monolayers (SAMs) open routes to new dielectric and conductor schemes. SAMs composed of sub-1nm organic chains and terminated with desired functional groups can help engineering thin-film dielectric and metal interfaces, and can strongly inhibit interfacial diffusion. Zsolt Tokei: “The use of SAMs has been a topic of research for the past ten years.”

“We have now moved this promising concept from lab to fab, and combined SAMs with a barrier/liner/metallization scheme on a full wafer.”

“Our researchers investigated the implications on the performance and scaling ability of this process flow. They demonstrated a ~18% reduction in the RC of 22nm half-pitch dual damascene interconnects, due to a better interface and thinner barrier.”
For conventional BEOL metallization, a barrier layer is coated by a Cu seed barrier, and this structure is electroplated with low-resistive Cu, which acts as the conductor. But when moving to sub-10nm interconnects, the resistivity of Cu continues to increase. At the same time, the diffusion barrier – which is highly resistive and difficult to scale – is taking up more space, thereby increasing the overall resistance of the barrier/Cu structure. Zsolt Tokei: “We are therefore investigating alternative metals that could possibly serve as a replacement for Cu and do not require a diffusion barrier. Among the potential candidates, such as Co, Ni, Mo, etc., platinum-group metals, especially ruthenium (Ru), have shown great promise due to their low bulk resistivity and resistance to oxidation. They also have a high melting point which can result in better electromigration behavior.”

“Our team has realized Ru nanowires with 58nm$^2$ cross section area. The nanowires exhibit low resistivity and robust wafer-level reliability. For example, a very high current carrying capacity with fusing currents as high as 720MA/cm$^2$ was demonstrated.”

![Graph showing the time dependent behavior of Ru nanowires under thermoelectric stress](image)

*Time dependent behavior of Ru nanowires under thermoelectric stress*
At the 2017 IITC conference, Zsolt Tokei was invited to take part in a panel discussion, organized by Applied Materials, to discuss the latest developments in metallization at single-digit nodes, the challenges and bottlenecks arising at these very small dimensions, and new application-driven requirements. Distinguished speakers from the technical field reviewed viable solutions for extending the current technology and alternative options were discussed. Zsolt Tokei: “From the discussion it is clear that the biggest immediate benefit can be found in the area of conductors – both from the material side as well as design. Indeed, it is driving the replacement of copper at specific metallization levels. Other avenues – such as dielectric innovations, functionality in the BEOL or 2D materials – remain interesting options for the R&D pipeline.” As an option that is further out, spin wave propagation in conductors is an alternative signaling to traditional electron based propagation.

Adding additional functionality in the BEOL

In the future, more and more technology options may get dictated by the requirements of systems or even applications.

“This could result in a separate technology for e.g. high-performance computing, low-power mobile communication, chips for use in medical applications, or dedicated chips for IoT sensors.”

Along the same lines, imec is investigating the benefits of introducing additional functionality in the BEOL.

Zsolt Tokei: “More specifically, we are evaluating the possibility of integrating thin-film organic transistors – with typically low-leakage level – into the BEOL interconnect circuitry of Si FinFETs. The potential advantages of fabricating them together are mainly a reduced power consumption and improved area saving.” A variety of circuits can fully utilize the benefits of this hybrid processing, including portable applications, eDRAM, displays and FPGA applications. Zsolt Tokei: “As a concrete example, we are currently merging imec’s expertise in BEOL technologies and in thin-film-based flat panel displays, thereby opening opportunities for new applications...”

Want to know more?

- Zsolt Tokei also presented this topic at the imec technology forum (ITF) 2017 USA. Do you want to be present at one of our ITFs, please check the ITF website
- This article is a compilation of 4 IITC papers. If you would like to receive these papers, please contact us via imecmagazine@imec.be
Biography Zsolt Tokei

Zsolt Tokei is Distinguished Member of Technical Staff Interconnects at imec. He joined imec in 1999 and since then held various technical positions in the organization. First as a process engineer and researcher in the field of copper low-k interconnects, then he headed the metal section. Later he became principal scientist, Program Director Nano-Interconnects and, in 2016, was appointed Distinguished Member of Technical Staff Interconnect. He earned a M.S. (1994) in physics from the University Kossuth in Debrecen, Hungary. In the framework of a co-directed thesis between the Hungarian University Kossuth and the French University Aix Marseille-III, he obtained his PhD (1997) in physics and materials science. From 1998 he worked at the Max-Planck Institute of Düsseldorf, Germany, as a post-doctorate researcher. From the date of joining imec he continued working on a range of interconnect issues including scaling, metallization, electrical characterization, module integration, reliability and system aspects.