Semiconductor technology & processing, Internet of Things

Towards improved data retention in OxRRAM memory devices

Imec researchers designed and fabricated an optimized TaOx/Ta stack with largely improved retention.

OxRRAM memory, a class of resistive RAM devices, has already shown its potential for embedded Internet-of-Things devices. The technology is highly scalable, reliable and simple to process. OxRRAM memories are however not yet mass produced, and this is mainly due to a poor understanding of the data retention failure mechanisms. Imec scientists have investigated for the first time the impact of both programming history and oxide-metal interface on OxRRAM data retention. The results of this study have enabled them to design and fabricate an optimized TaOx/Ta stack with largely improved retention. They presented their results at the 2016 IEDM conference*.

Resistive RAM, a promising candidate for embedded memory applications

Resistive random access memory – or RRAM – has emerged as a promising candidate for embedded memory applications. The devices can potentially be fabricated at low cost and allow operation at low voltage, making them especially attractive for Internet-of-Things applications. An RRAM device in general relies on the formation of a conductive filament in a thin dielectric layer that is sandwiched between two electrodes. When an electric field is applied, the ionic movements and structural changes in this insulating medium cause a measurable change of the device resistance. Memory operation makes use of two different resistance states: high resistance state (HRS) and low resistance state (LRS). Switching from one to the other can be done by applying an appropriate electric field. The operation which changes the resistance for HRS to LRS is called a 'set' process, while the opposite is defined as 'reset'. The specific resistance state (HRS or LRS) can be retained after the electric field is switched off, and this indicates the non-volatile nature of the RRAM memory.

OxRRAM, challenged by data retention

In the OxRRAM-type of memory, the filamentary switching is based on oxygen vacancy migration in transition metal oxides. The technology shows excellent scalability and reliability, and can be fabricated by using a simple integration flow. However, the mechanisms causing data retention failure are not completely understood, and this hinders widespread adoption of the technology. In particular in low-current and fast-pulse programming regimes, a small population of fast-erasing bits (also called retention tails) typically appears. Imec previously associated these retention tails to excess mobile oxygen ions. During set/reset cycling, these oxygen ions can be injected in or removed from the conductive filament. When the set pulse is insufficient to remove these excess ions from the filament, the ions recombine with oxygen vacancies, and this results in retention failure.

The imec researchers have now extended this analysis by studying the impact of the program history on the data retention properties of the tail bits. In addition, they investigated the role of the oxide-metal interface in improving the data stability in OxRRAM devices.

An innovative method for retention assessment

The scientists used an innovative and cost-effective method for statistically investigating the data retention. Conventional assessment methods are performed on a device-by-device-basis, assuming that retention failures due to fast erasing bits are related to device-to-device differences – arising from e.g. variation in the processing of the memory device. Imec however assumed that the origin of the excess ions is related to inherent variations in the cycle-to-cycle set/reset programming. Therefore, to assess retention, a single OxRRAM cell (instead of an array of cells) is now being programmed (set), sampled, and reprogrammed (reset) at retention baking temperatures, and this cycle is repeated at least 1500 times. This method is called single-cell cycle-to-cycle retention technique.

OxRRAM test devices

OxRRAM crossbar cells were integrated on top of a transistor in a so-called 1-transistor-1-resistor (1T1R) configuration. A 5nm thick HfO2 layer (the dielectric) is sandwiched between a 30nm TiN bottom electrode and a Hf (10nm)/TiN top electrode. The overall device size is 40nmX40nm. This TiN/HfO2/Hf stack is used to evaluate the impact of programming conditions. Different stacks were fabricated to investigate material engineering solutions, such as the role of the oxide-metal interface.
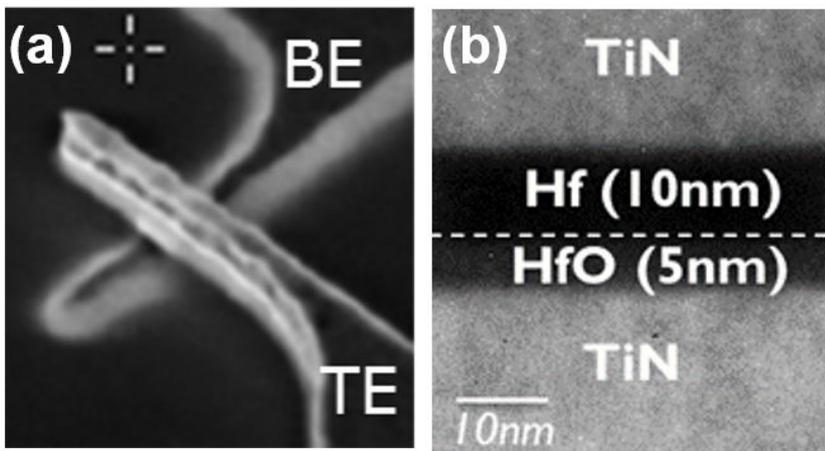
(Left) OxRRAM crossbar cell and (right) cross-sectional TEM image of the TiN/HfO2/Hf device.

The impact of program history and metal-oxide interface

The researchers found for the first time that the retention in the LRS state is largely dependent on the program history of the memory cell. For example, the use of a short reset pulse of high amplitude in combination with a long set pulse can largely improve LRS retention. They also showed that it is possible to clean excess O-ions by iterating short set/reset cycles. Also, the delay time between set and reset pulses plays an important role. When set programming is applied immediately after reset, worse retention is obtained compared to cases with some delay. In practice, this means that smart writing algorithms will be needed to avoid writing the same bit repetitively in a short time. For the HRS in a HfO2/Hf stack, experiments suggest that HRS retention failure is not governed by the concentration of remaining O-ions in the conductive filament. The results have been supported by modelling (i.e., hourglass retention simulations).

In addition, material engineering solutions were proposed to improve the data retention. The experiments were based on an earlier presumption that the retention strongly depends on the oxygen chemical potential profile (more specifically, the asymmetry of the profile) along the conductive filament. To prove this, an OxRRAM stack was made in which the Hf electrode was replaced with a Ti cap, exhibiting a worse chemical profile asymmetry. It was shown that Ti capping indeed gives worse data retention. Therefore, a stack with optimized chemical potential profile is highly desirable.

An improved OxRRAM stack for embedded applications

These experimental and modelling efforts have greatly enlarged the understanding of OxRRAM data retention failure mechanisms. The results have allowed the imec researchers to propose an optimized OxRRAM stack, based on a TaOx/Ta system with ideal chemical potential profile. The new stack, in combination with an optimized programming sequence, shows much better data retention compared to the HfOx-based OxRRAM cell, for both the LRS and HRS states. The results were confirmed by conventional device-to-device retention tests. The new cell is also compatible with back-end-of-line thermal stress.
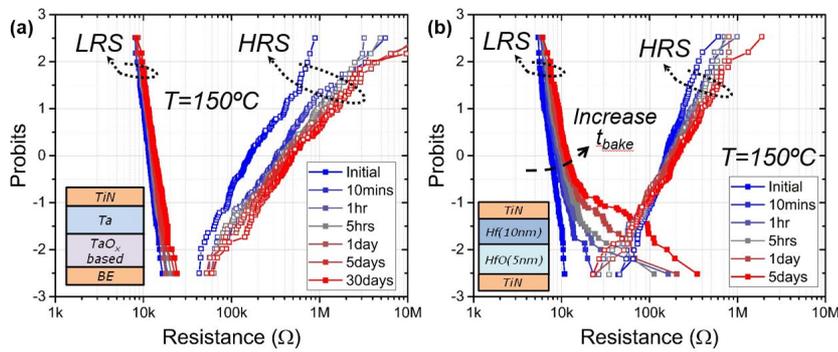
Long-term retention test (device-to-device) up to 30 days on (a) a TaOx-based stack for embedded application and (b) a reference HfO2-based stack. The results show improved data retention, in both the LRS and HRS state, for the optimized TaOx-based stack.

* 'Statistical investigation of the impact of program history and oxide-metal interface on OxRRAM retention', C.Y Chen (imec and KU Leuven); A. Fantini, R. Degraeve, A. Redolfi, G. Groeseneken, L. Goux and G.S. Kar (imec), 2016 IEDM conference