Semiconductor technology & processing

When logic goes democratic

The potential of spintronic and plasmonic majority gates.

Intro

While CMOS device scaling is being pushed to its ultimate limits, researchers at imec are also exploring alternative solutions that break away from the fundamentals of classical scaling. They are looking into disruptive technologies that could reduce cost, limit power consumption, optimize performance per circuit area or allow for very high operation throughput. With these technologies, they do not aim to replace CMOS circuits, but rather complement them in a hybrid, multi-device architecture. In these architectures, the new technologies will be used to do what they are good at, e.g. high-performance computing, or ultralow-power operation.

One of these 'beyond-CMOS' options are majority gates, a paradigm-shifting technology that completely changes the way we build circuits. In conventional computational circuits, complex logic operation is performed through combinations of several NAND gates. In NAND-based logic, an output is false only if all its inputs are true. In hardware, the NAND gates are implemented using transistors. Majority gates are 'democratic' devices that return true if more than 50% of their inputs are true. In their most simple implementation, they use three inputs and one output. If, for example, two inputs are in a true state ('1') and a third one is in a false state ('0'), the expected state at the output is true. This majority gate operation can be summarized in a truth table, listing all possible configurations of the input variables (i.e., '1' and '0') together with the result of the operation of those values.

Majority Logic Gate			
Input 1	Input 2	Input 3	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Truth table of a simple '3 input 1 output' majority gate.

With these majority gates, logic AND and OR operations can be emulated. They enable arithmetic circuits that promise to be much more compact and energy efficient than the conventional NAND-based circuits.

Although majority gates can be built using standard transistors, more efficient devices could be made by incorporating other concepts. The imec team is investigating and benchmarking three different implementations of majority gates: spin-wave majority gates, spin torque majority gates and plasmonic majority gates. They differ in the way the information is encoded and processed in the device, and in the way the information is converted from the classical circuits based on transistors to these novel devices. This brings along different challenges, but also gives each of the devices distinct advantages – in terms of speed, power and area consumption, or in the ease with which circuits can be built.

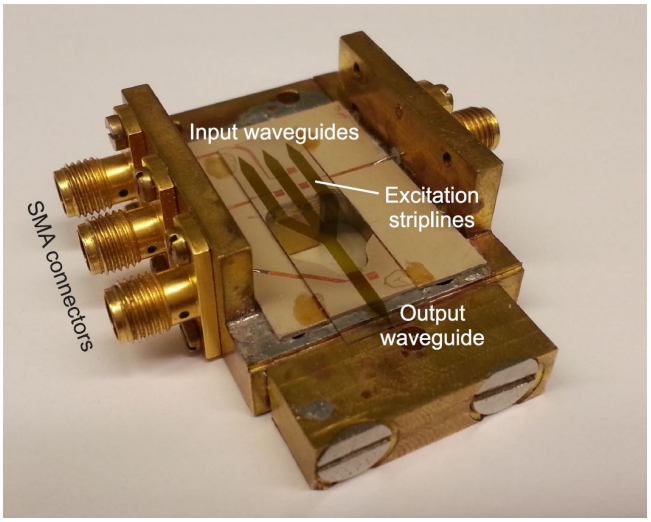
Below, Iuliana Radu and the imec exploratory device team review the status of the three different majority gates.

Spin-wave majority gates: compact and ultra-low power

Spin-wave majority gates belong to the family of spintronic devices, which exploit the collective magnetization state in a ferromagnet rather than the charge of individual electrons to perform logic operations. In a magnetic material, the magnetization can oscillate, creating nanoscale waves of magnetization that propagate, the so-called spin waves or magnons. Spin waves have wavelengths in the micrometer to nanometer range and frequencies in the gigahertz (GHz) to terahertz (THz) range. Majority gate operation relies on the interference of (at least) three of these spin waves. The information can be encoded in either the amplitude or the phase (0 or π) of the waves. Using the phase to encode information is the most natural way leading to majority gates, since the phase of the wave after interference is simply the majority of the phases of the individual waves before interference.

Spin-wave majority gates promise a significant area and power reduction per computing throughput. Let's take the example of a one-bit adder, a circuit that performs the addition of two binary bits. In CMOS technology, building such a circuit requires about 25 transistors. An equivalent wave computing circuit only requires 4 waveguides and 5 transducers to perform the same operation – transducers being the components that bridge between CMOS and the spin-wave domain. When benchmarking the spin wave majority gates against CMOS circuits by using micromagnetic simulations, imec concluded that the spin-wave circuits take on average 400 times lower power and 3.5 times less area than their CMOS counterparts.

Experimental validation of majority gate operation was lacking until recently - when researchers at the Technical University of Kaiserslautern in Germany, in collaboration with the imec team, demonstrated a first prototype of a spin-wave majority gate [1]. This first prototype is bulky and required the use of a material that is difficult to process industrially: yttrium iron garnet. However, the device fulfils the basic description of such a majority gate. The logic information is encoded in the phase of the input spin waves while the phase of the output signal represents the majority of the three phase states of the spin waves in the three inputs.

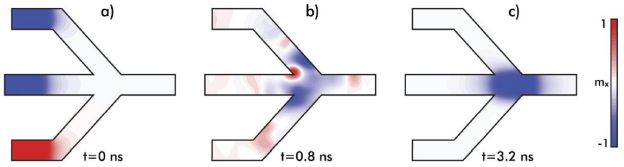


Large-scale prototype of a spin-wave majority gate.

The imec team is currently working on scaling down the spin-wave majority gate devices towards the few nanometer range. The scaled devices would also require efficient transducers. Therefore, the imec team is actively researching components as spin-wave transducers, based for example on spin-orbit torques or the magnetoelectric effect. Transducers based on the magnetoelectric effect consist of piezoelectric and magnetostrictive

ferromagnetic layers and couple voltage signals to magnetic ones via strain as the intermediate link. Such magnetoelectric transducers promise to operate efficiently for devices in the sub-micrometer range. The targeted dimensions, sub-micrometer, and the resonance frequencies in the GHz range bring these piezoelectric actuators to the frontier of nano-electromechanical systems (or NEMS) research.

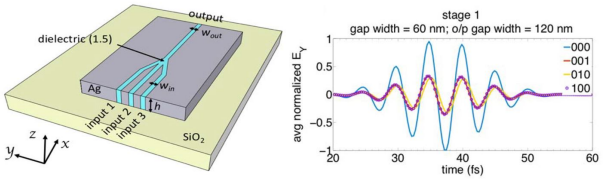
Recently, imec proposed based on modeling, the first nanoscale design of a spin-wave majority gate with a total area of 0.05□m^2 utilizing magnetoelectric cells (as shown in the figure below). Imec is now working towards an experimental demonstration. In recognition of how ambitious this project is, a European multi-national consortium formed by nine research teams and coordinated by imec has been awarded an EU Horizon 2020-FET-Open research grant, CHIRON, to help demonstrate these devices.



Simulation of the operation of a nanoscale spin-wave majority gate. (a) At t=0ns, the inputs are set to '110'; (b) at t=0.8ns; and (c) at t=3.2ns, the output magnetization is stabilized to the '1' state, correctly detecting the majority result. Total area of the device is about 0.05□m^2.

Plasmonic majority gates: speed champions

Recently, a novel type of wave-based majority gates has gained attention: the plasmonic majority gate. In these devices, the key actors are plasmons which can be thought of as waves in a metal's free electron gas. These waves propagate in plasmonic waveguides (nothing other than insulating materials sandwiched between metal stripes), which can be used as the building blocks for majority gates. For a sketch of a plasmonic majority gate, see the figure below. Similar to spin waves, the plasmonic majority gate operation is based on the interference of the propagating plasmons. They carry the information in their phase, at frequencies exceeding THz – which is about three orders of magnitude faster than CMOS-based electronics. Although less energy efficient, they show tremendous potential for high-throughput computation and ultrafast operation.

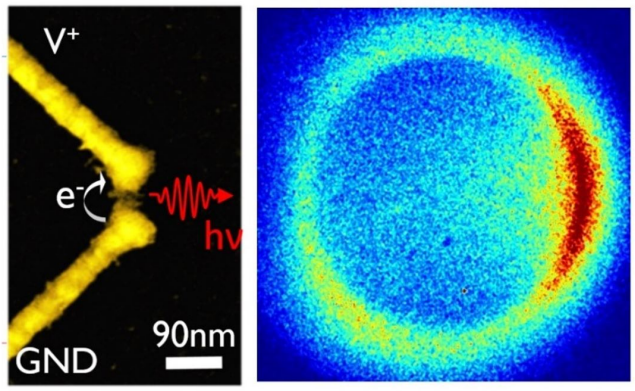


Plasmonic majority gate: (left) schematic representation and (right) output of a single stage majority logic gate displaying the results for the case of majority logic 0.

Recently, imec researchers in collaboration with Georgia Institute of Technology, USA have designed plasmonic majority gates based on electromagnetic simulations [2]. A single stage majority gate produces the output at an extremely low delay of only 50 fs, orders of magnitude faster than conventional transistor-based logic. When building logic circuits, a must-have is the ability to cascade devices and have the computation propagate from one

stage to the next. The proposal includes three levels of cascading stages without significant loss of the plasmon field intensity, a first of its kind.

One of the main experimental challenges for plasmonic majority gates is to excite and inject plasmons into plasmonic waveguides, and to do this 'on chip'. Imec is actively working towards such a device. Recently, an on-chip plasmon source has been experimentally demonstrated. This source is ultra-fast, compatible with high throughput computation [3]. At the heart of this plasmon source, there is an antenna-coupled tunnel junction (see figure below) which converts tunneling electrons into plasmons in a fully controllable way. The device features both passive and active tunability, and is capable of unidirectional light emission. The team is now working on coupling these devices to plasmonic waveguides and injecting propagating waveguide modes with minimum injection loss.



(Left) Imec's ultra-small antenna-coupled tunnel junction demonstrating unidirectional light emission (right).

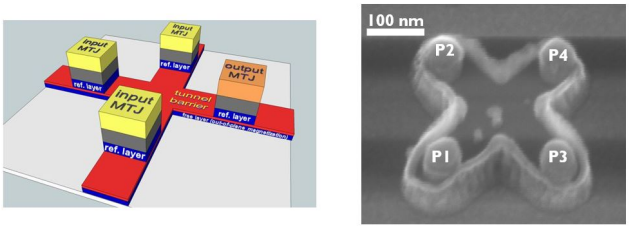
The road towards a full plasmonic majority gate experimental demonstration is, however, long and challenging. One of the major missing components today is a circuit that allows to convert the analog output signal from the wave-based circuits to a digital signal that is compatible with regular CMOS-based circuits. This analog-to-digital converter should also enable down-conversion from THz, the operation frequency of the plasmonic circuit, to GHz, the operation frequency of standard CMOS, and do this at the lowest possible energy.

Spin torque majority gates: easily 'cascadable'

Just like spin-wave majority gates, spin torque majority gates belong to the spintronic device family. In a spin torque majority gate, the information is encoded in magnetic domain walls – interfaces that separate regions with different magnetization direction. Based on quantum interactions between electrons (known as exchange), the domain walls propagate and interact, and the majority magnetization direction wins.

The majority gate itself consists of a cross-shaped free layer that is common to 4 magnetic tunnel junctions (3 inputs, 1 output). The magnetization direction of the 3 'input' free layers is switched using spin transfer torque, provided by a current through each of the magnetic tunnel junctions. The output state is measured via tunneling magnetoresistance.

Previously, the imec team validated functioning of spin torque majority gates through micromagnetic simulations. Meanwhile, first devices have been built on 300mm wafers (see figure below), and part of the truth table has been demonstrated. Based on materials and process optimization, it is expected that full device function will be soon demonstrated.



Spin torque majority gate: (left) schematic representation and (right) integrated device.

In general, spin torque majority gate circuits are compact and could target low-power operation. However, compared to spin-wave based operation, they consume more energy. A major advantage of spin torque majority gates compared to wave-based circuits is the 'ease' with which circuits can be designed. Circuits are typically made up of multiple computational stages, and cascading between devices, as mentioned above, has to happen in order to build meaningful logic circuits. In hardware, this means that the output of one set of devices goes to the input of the next stage of devices. Wave-based majority gates rely on the interference of waves, and these waves can easily flow back into the circuit. And this makes the design of 'cascadable' circuits very challenging. Spin torque majority gate operation relies on the interaction between domain walls. Domain walls are less likely to be channeled back into the device. Based on modeling, imec has proposed special implementations which reduce this effect even further.

Conclusion

In this article, we have reviewed the status, challenges and benefits of three types of majority gates: spin-wave majority gates and plasmonic majority gates – both wave-based computational circuits – and spin torque majority gates. With these beyond-CMOS technologies, low-power and compact arithmetic circuits can be built, that completely change the way we build logic circuits. Once mature, they are envisioned to perform, in a hybrid architecture, specific functions – depending on their individual strengths. While spin-wave based majority gates promise to be compact and ultralow power, the main asset of the low-power spin torque majority gates is the ease with which multiple-stage circuits can be built. On the longer term, plasmonic majority gates have the potential to be used for applications that require extremely high throughput and speed, and for which energy efficiency is a second consideration.

Acknowledgements

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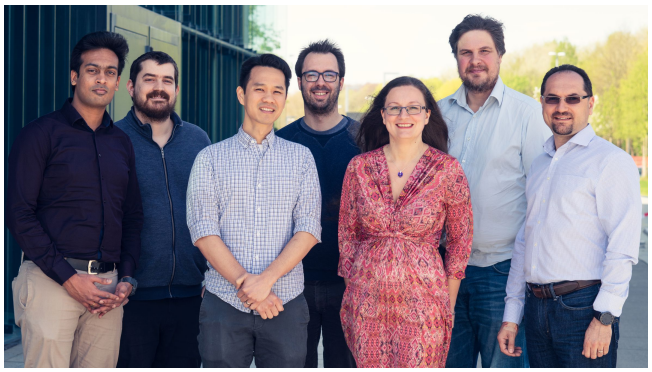

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[2] 'Proposal for nanoscale cascaded plasmonic majority gates for non-Boolean computation', Dutta S. et al., Scientific Reports 2017, 7, 17866
[3] 'Electrically driven unidirectional optical nanoantennas', Gurunarayanan S. et al., Nano Lett. 2017, 17, 7433−7439

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Biography Iuliana Radu

Iuliana Radu is Distinguished Member of Technical Staff at imec, where she is leading the Beyond CMOS activities. Prior to joining the Logic Program at imec in 2013, she was a Marie Curie and FWO fellow at KU Leuven and imec. Her work at imec and KU Leuven includes devices using the metal to insulator transition, ionic and electronic transport in functional oxides and devices with graphene and other 2D materials. Iuliana has received a PhD in Physics from MIT in 2009 where she worked on the Fractional Quantum Hall effect and searched for non-abelian quasiparticles. She has received a MSc and a BSc in Physics from University of Bucharest.