General

Preface November 2018

Each month our CEO reflects on the events in his (professional) life and discusses some of the articles featured in the magazine. This month he tells us about the visit paid by the program partners to imec and the new collaboration with ASML on upscaling EUV lithography and on High-NA lithography, the technique par excellence for producing even better chips.

“Imec and ASML have been partners for almost 30 years now and the new work we are doing together on upscaling EUV lithography and developing the next generation of High-NA EUV lithography is of great importance for all our partners with whom we are building the chips of the future.”

October is typically a busy month at imec. Twice each year – one of which is in October – around 700 employees from our program partners pay us a visit at imec. While they’re here, things are really buzzing in the various imec buildings and meeting rooms. It makes for an inspiring hubbub, too, because it provides the ideal opportunity for us all to sit down together again, discuss the results that have been achieved and set out our plans for the future. And for our researchers, it always provides a great incentive to finish their tests, process their results and decant it all into a fine-looking presentation.

On day one of this latest ‘Partner Technical Week’, we announced an exciting new collaborative project with ASML. First and foremost this will involve working more closely with ASML to prepare EUV lithography for higher production volumes in the chip industry. Then, in parallel, we will also be working on the next generation of EUV lithography needed to make the basic building blocks of chips and transistors even smaller and hence enable us to build even more powerful chips than is possible at the moment. This research will be carried out on a new EUV lithography tool with a higher numerical aperture (NA).

Of course we can’t really call our collaboration with ASML ‘new’. After all, we have been partners for nearly 30 years and the success of our core CMOS (chip scaling) partner program can be attributed to a large extent to our working together. One great benefit is that it enables us to have the most advanced lithography equipment in our cleanroom at all times, where material and equipment suppliers can work with chip manufacturers on the technology and production techniques for the chips of the future.
The chip industry and research centers such as imec are always on the lookout for new ways of making chips better. This may be by downscaling the chip structures. But there are other ways, too, such as supervias. Supervias are a sort of ‘shortcut’ in the interconnection layer that connects transistors to each other. They enable signals to pass through the chip more quickly. More about these supervias elsewhere in this imec magazine.

This magazine also contains great stories about how imec is working with psychiatrists to treat depression and autism; how the PV industry will be organized totally differently in the future; what our JPEG research has to do with major artworks; how one of our spin-offs makes assessing pupils more objective; and how we will be giving your TV evening a whole new dimension.

Happy reading!

Luc Van den hove,
President and CEO imec