Semiconductor technology & processing

Guido Groeseneken on transistor reliability

“Our research into transistor failure mechanisms has led to self-learning chips, new data security technologies and new biosensors”

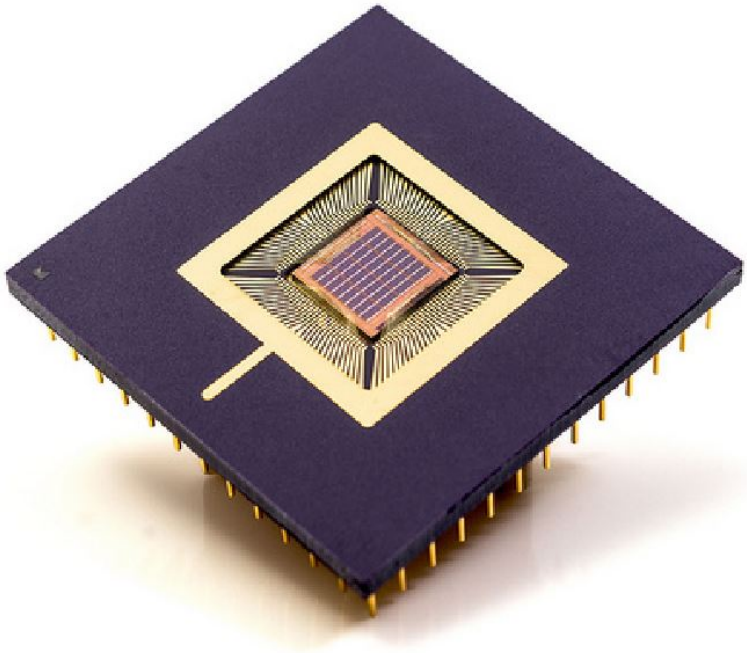
Guido Groeseneken, imec fellow & expert in the reliability of transistors and electrical characterization

To be able to guarantee the reliability of transistors, we have been conducting research for some years now at imec to see what happens when transistors operate properly and when they fail. We’ve been doing this in terms of circuits, devices and materials – and sometimes right down to the level of atoms. The insights that we gather from this work help us to provide the right feedback to the process technologists, who in turn are able to make the transistors more reliable. It is particularly interesting to note that in recent years the knowledge we have gained about these failure mechanisms can also be applied to other areas. These insights no longer only serve to solve problems, but are the basis for innovative and surprising solutions in very diverse domains.

Last year, imec spent a lot of time working on self-learning chips, data security codes, FinFET biosensors and computer systems that can correct themselves. These are innovations that draw on the knowledge present in imec’s reliability group.

Self-learning chips

For example, take the self-learning or neuromorphic chip that gave imec such extensive coverage in the media in 2017. The development of this chip is based, among other things, on our knowledge of “resistive RAM” or RRAM memories, which use the breakdown of an oxide to switch a memory bit on or off (0 or 1). This oxide breakdown – which was previously (and still is) a reliability problem – occurs because a conductive path is created through the oxide, known as a filament. However, the work conducted by imec’s reliability group has demonstrated that not only can you create a filament or make it disappear, but that there are intermediate levels as well, which means that the strength of the filament can be controlled. And that is precisely what happens in our brains: the connections between neurons can become stronger or weaker according to the occurrence they are processing or the learning process they use, etc. This means that these RRAM filaments can be used in chips that work like our brains. It was this insight that provided us with the foundation for the development of imec’s neuromorphic chip, which – as has been demonstrated – can even compose music.



Imec's neuromorphic chip, developed by researchers from both the reliability group and the computer architecture group.

Data security

Since recently we are also working closely with COSIC, an imec research group at KU Leuven that specializes in computer security and cryptography. Also here we can draw on our knowledge of transistor breakdown mechanisms. These can be used to create and read out a fingerprint that is unique for each chip and that cannot be predicted, hence the name 'physically unclonable functions' (or PUFs). This unique fingerprint makes it possible to ascertain the identity of chips in data exchanges and thus to prevent hacking by means of rogue chips.

The phenomenon of 'Random Telegraph Noise', which has long been known in the area of transistor reliability, could also be used as a security fingerprint. Random telegraph noise is a name for sudden jumps in voltage or current levels as the result of the random trapping of charges in traps within the gate insulation of a transistor. This phenomenon is unpredictable and random, and hence it could also be perfectly usable as PUF.

> *What was once a problem for us – the breakdown of oxides or the existence of random telegraph noise – is now at the base of major new solutions for computer security.*

Biosensors

A third example of discipline-overlapping innovation brings us to the world of life sciences. FinFET transistors are essential for the current and future generations of computer chips. As a result of the research carried out in our group, we have now found out a great deal about the way they work, including their failure mechanisms, etc. So much so that we can now explore the possibility to use them as biosensors. What happens is that biomolecules have a certain charge and when that charge comes into the vicinity of a FinFET, the current in the FinFET will be influenced. As a result, there is the potential that the presence of a single biomolecule can be detected by such a FinFET

Self-healing chips

And, finally, we are also working with system architects to produce reliable chips, even with transistors that are no longer reliable. Extremely small transistors with dimensions smaller than 5 nanometers can be very variable and the way they behave is unpredictable. For that reason we are working with system architects on solutions such as self-healing chips, based among other things on the existing models of the failure mechanisms that we provide them with. These self-healing chips will contain monitors that detect local errors. A smart controller then interprets this information and decides how to solve the problem, after which actuators are directed by the controller to carry out the task required.

What about scaling?

Numerous methods are currently being investigated to ensure that transistors can still be miniaturized and improved for as long as possible, as propounded in Moore's Law. To do so, the classic transistor architecture has already been replaced by a FinFET architecture and in the future this will evolve even to nanosheets or nanowires. Materials other than silicon, with greater mobility, are also being looked at, such as III-V materials (germanium for pMOS and InGaAs for nMOS).

In the choice made for these future architecture, it is extremely important to also look right from the start to the failure mechanisms and reliability of the new solutions. As an example, last year, our reliability team focused extensively on III-V transistors. Although these transistors score well in terms of mobility, their stability is still one of the main challenges remaining before we are able to take the next step and start manufacturing. The insulation layers in III-V transistors contain a lot of traps that cause this instability in transistor characteristics. Understanding this phenomenon is essential if we are to find a solution for it. So, a breakthrough in this area is needed urgently and our results, which were published in a recent IEDM paper, are certainly a step in the right direction. In the invited paper by Jacopo Franco these instabilities are first analyzed in detail. Then, based on this analysis, practical guidelines are given for the development of III-V gate stacks that offer sufficient reliability.

It's very difficult to look ahead even further into the future, because as the end of Moore's Law approaches, increasing numbers of different technologies and concepts are already on the radar (quantum computers, 2D materials, neuromorphic computers, spinwave logic, etc.). However, none of these concepts has yet made a real breakthrough. But in my view 2017 was the year in which the industry began to take a strong interest in quantum computers, with major investments from important players such as Google and Intel. Imec also plans to play a major role in this field, with the launch of a new program on quantum computing, gathering the extensive expertise available. In the past, quantum computing has been considered more as a purely academic field of research – something of value for physicists at universities, but not for engineers and companies. So perhaps the breakthrough of industrial quantum computing will be the next milestone in the history of electronics. Or perhaps this milestone will come from a totally unexpected angle – by combining knowledge and people from entirely different disciplines, creating totally new ideas and concepts. Only the future will tell us!

Want to know more?

- Read the press release about the neuromorphic chip
- Read the article in imec magazine about self-healing chips
- Ask for the invited IEDM paper about the reliability of InGaAs via this link

Biography Guido Groeseneken

Guido Groeseneken received his M.Sc. in Electrical and Mechanical Engineering (1980) and Ph.D. in Applied Sciences (1986), both from the KU Leuven, Belgium. In 1987 he joined imec, where he is now acting as scientific fellow, covering research fields of advanced devices and reliability physics of sub-10nm CMOS technologies. He is also Program Director of the imec PhD program and Director of Academic Relations.
He has been a part-time Professor at the KU Leuven since 2001, where he has managed the European Erasmus Mundus Master program in Nanoscience and Nanotechnology from 2005 to 2017. In January 2005 he was elevated to the rank of IEEE Fellow. Guido has been a member of the Technical Program Committee for several international scientific conferences, including the IEEE International Electron Device Meeting (IEDM), the European Solid State Device Research Conference (ESSDERC), the IEEE International Reliability Physics Symposium (IRPS), the IEEE Semiconductor Interface Specialists Conference (SISC) and the EOS/ESD Symposium. From 1999 until 2006 he acted as an editor of IEEE Transactions on Electron Devices. He is the recipient of the 2017 IEEE Cledo Brunetti award.