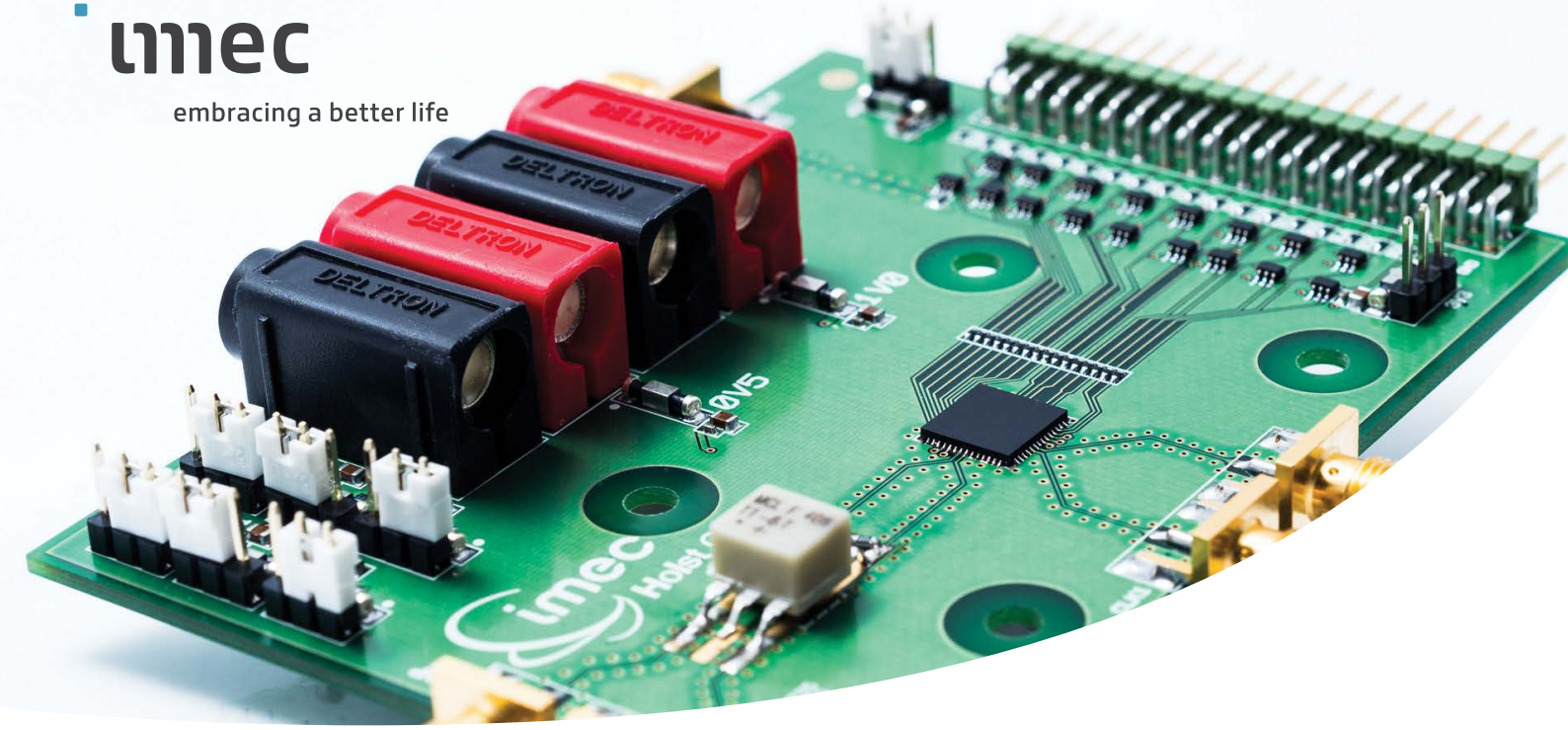
imec

embracing a better life



13BIT SAR ADC FOR ULTRALOW-POWER WIRELESS SENSOR NODES

DESCRIPTION

This ADC has 13bit resolution and can support sample rates from DC to 6.4MS/s at 1.0V. It successfully implements a low-power fully automated on-chip background calibration that utilizes a redundancy facilitated error-detection and correction scheme for the DAC mismatch and comparator offset.

Thanks to the low-power calibration, this ADC achieves an ENOB of 10.4b and a state-of-the-art power-efficiency of 5.5fJ/conv.step at 6.4MS/s.

MEASUREMENT RESULTS

Technology	40nm
Resolution	13bit
Chip area (mm^2)	0.0675
Input capacitance (pf)	1.3
Inl (lsb)	3.79
Dnl (lsb)	1.08
Supply (v)	1.0
Common-mode level (v)	0.4
Sampling rate (msps)	6.4
Input signal range (vpp-diff.)	1.65
Power consumption (µw)	46
Leakage (nw)	<140
Enob at nyquist (bit)	10.4
Fom (fj/conv. Step)	5.5

KEY FEATURES

Low-power techniques

- Asynchronous dynamic logic
- Two-mode comparator
- Low-power calibration

Excellent performance

- Power consumption: 46µW @ 1.0V supply
- FoM: 5.5fJ/conv.step @ 1.0V
- Leakage <140nW @ 1.0V
- Dynamic power from 0 to 6.4MS/s

Low-cost calibration

- Fully on-chip background calibration
- Little overhead in power, speed or area

APPLICATIONS

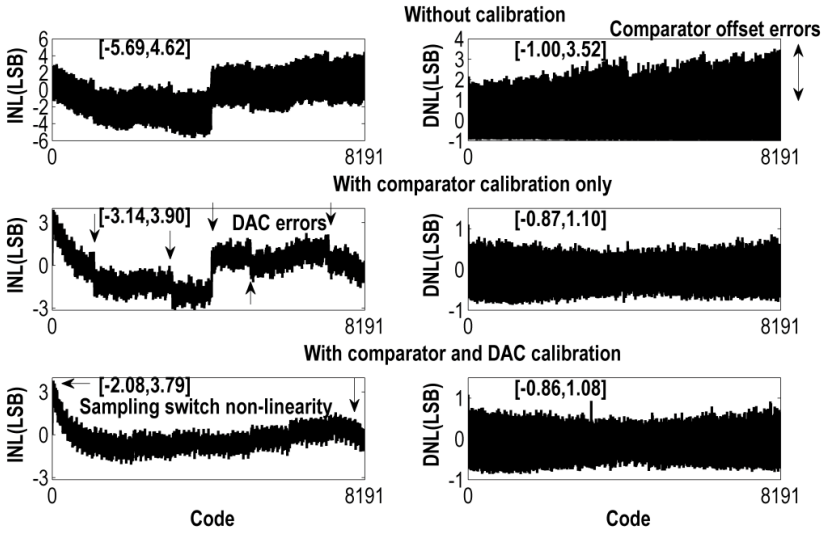
- Wireless sensor nodes

EVALUATION BOARDS

Imec provides evaluation boards (EB) on request to prospective customers and partners interested in licensing imec's radio designs & IP.

STATIC PERFORMANCE

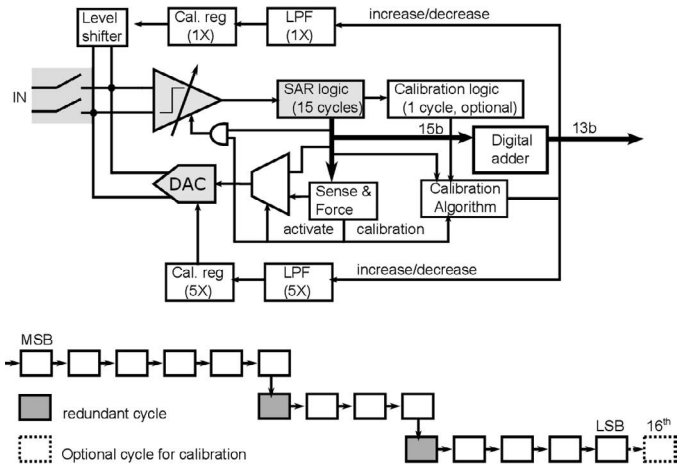
All measurements are performed at 1V supply. The INL and DNL after calibration are 3.791LSB and 1.08LSB at 1V. The calibration suppresses the large initial DNL/INL errors due to the comparator offset and the DAC mismatch. The remaining non-linearity is due to the sampling switch.



BLOCK DIAGRAM

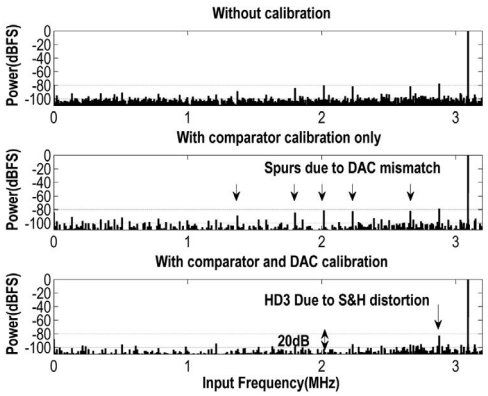
A total of 15 cycles is used to perform a 13b conversion, where the 7th and 11th cycle are redundant cycles. The redundancy relaxes DAC settling requirements, enables the proposed background calibration and saves power using a two-mode comparator: the comparator works in low-power mode first and switches to high-precision mode in the latter cycles, resulting in 2x energy reduction.

The automated background calibration can suppress both DAC mismatch and comparator offset errors with negligible overhead in area or power. The calibration can be running in the background without interrupting the ADC operation.



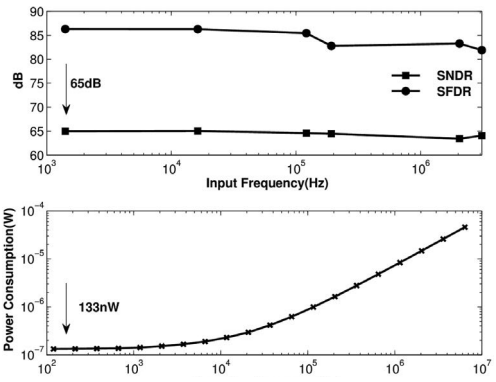
FREQUENCY SPECTRUM

The spectrum with a near Nyquist-tone is shown in three scenarios. Spurs, due to the comparator offset and DAC mismatch, are effectively reduced to a low level.



DYNAMIC PERFORMANCE

The ADC achieves 10.4bits while consuming 46µW at Nyquist frequency at 1.0V supply and 6.4MS/s, resulting in 5.5fJ/conv.step FoM. The power efficiency is maintained over sampling rate.



AMERICAS
raffaella.borzi@imec.be
T +1 408 386 8357

CHINA
timo.dong@imec-cn.cn
+86 13564515130

EUROPE & ISRAEL
michel.windal@imec.be
+32 478 96 67 29

JAPAN
isao.kawata@imec.be
T +81 90 9367 8463

TAIWAN & SE-ASIA
mavis.ho@imec.be
T +886 989 837 678

VIETNAM, BRAZIL, RUSSIA, MID EAST, INDIA
max.mirgoli@imec.be
T +1 415 480 4519