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embracing a better life

EUROPRACTICE
IC SERVICE

GaN-ICs FOR MONOLITHIC INTEGRATION OF POWER SYSTEMS

To unlock the full potential of GaN power electronics, imec offers a unique GaN-on-SOI process. The deep-trench isolation implemented in this process provides full isolation between power devices, drivers, control and protection circuits. This, in turn, enables the manufacturing of complex GaN ICs. In addition to accommodating smaller form factors, the close proximity of devices drastically reduces parasitic inductance, resulting in a significant switching speed enhancement.

LOW-COST MPW AND DEDICATED MASK RUNS

To make GaN-on-SOI devices and circuits more affordable and easily available to its customers, imec offers a Multi-Project Wafer (MPW) service. In this MPW model, mask, processing and engineering costs are shared across multiple customer designs, typically delivering prototyping runs of 100 samples dies. For even larger quantities, dedicated mask runs can also be requested which return approximately 12 x 200 mm/8 inch wafers. For even larger productions runs, we offer the possibility of engaging with external manufacturing partners.

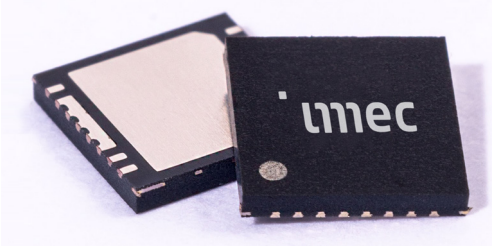
STATE-OF-THE-ART ENHANCEMENT MODE POWER DEVICES ON 200MM/8-INCH Si WAFER

Today, GaN-based power devices are mainly available as discrete components which have, nonetheless, been used to push both operating frequencies and efficiencies of Switched-Mode Power Supplies (SMPS) to record levels. The technology's full potential, however, has been difficult to unlock due to difficulties in reducing the parasitic inductances, the necessity of extremely fast turn-on times, and the low Cg/Cgd ratio. Solutions using discrete GaN power devices have therefore resulted in maximum switching speeds far short of their potential values.

Imec's GaN-on-SOI IC technology circumvents these limitations by allowing customers to monolithically integrate components such as half-bridge and GaN drivers onto the same die, minimizing parasitic inductance.

WITH IMEC'S GaN-IC TECHNOLOGY YOU ARE ABLE TO:

- Integrate multiple transistors on a single IC using trench isolation
- Save package cost by packaging one instead of multiple devices
- Reduce system parasitic inductance



Picture of the 5x5mm² 200V 15A packaged GaN device

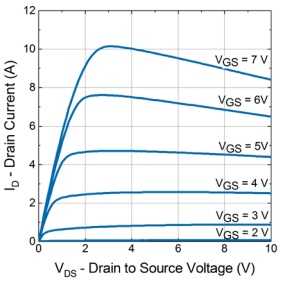
GaN-ON-SOI DESIGN KIT

To make this technology more easily available, imec provides an extensive GaN-on-SOI Process Design Kit (PDK). This kit includes process documentation, library devices, layout guidelines for custom design, verification and models. Low-ohmic and high-ohmic resistors are provided, as well as Metal/Oxide/Metal capacitors, temperature sensors and low voltage logic devices and logic gates (invertors, NAND, NOR, RS Flip-flops,...). These enable customers to design highly integrated GaN power systems on chip. The PDK is available after signing imec's GaN-IC Design Kit License Agreement (DKLA).

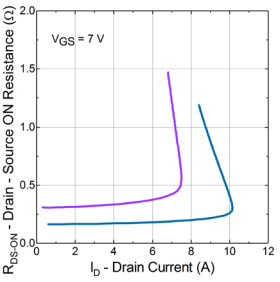
200 V e-MODE p-GaN HEMT

Datasheet Power Device with Weff = 36 mm

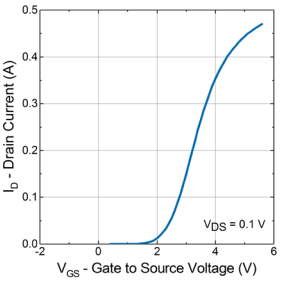
SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ABSOLUTE MAXIMUM RATINGS						
BV_{DS}	Drain-Source voltage				200	V
I_D	Pulsed Drain current	1 ms pulse			10	A
V_{GS}	Gate-Source voltage				7	V
ON/OFF STATE CHARACTERISTICS						
BV_{DS}	Drain-Source voltage	V_{GS} = 0 V, I_D = 1 µA/mm	200			V
I_{DSS}	Drain-Source leakage	V_{GS} = 0 V, V_{DS} = 200 V		0.5		µA
I_{GSS}	Gate-Source leakage	V_{GS} = 0 V, V_{DS} = 200 V		0.27		µA
R_{DS-ON}	Drain-Source ON resistance	V_{GS} = 7 V, I_D = 2 A		0.16		Ω
V_{TH}	Gate-Source voltage	maximum g_m		2.3		V
		V_{DS} = 0.1 V, I_D = 10 µA/mm		1.3		
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V V_{DS} = 200 V f = 1 MHz		55		pF
C_{OSS}	Output capacitance			35		pF
C_{RSS}	Reverse transfer capacitance			0.97		pF



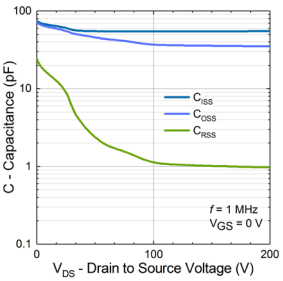
Typical IDS vs. VDS curve at T=25 °C



RDS vs. VDS(on) vs IDS at T=25 and 150 °C



Typical IDS vs. VGS curve at T=25 °C

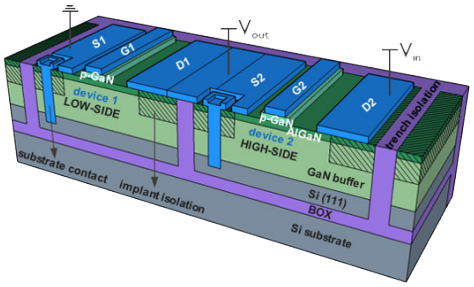


Typical CISS , COSS and CRSS vs VDS at T=25 °C
Measurements on-wafer (no packaging parasitics included).

MONOLITHIC INTEGRATION USING GaN-ON-SOI

Except for systems at low voltage (<50Volt), co-integration of low-side and high-side power devices is not possible using GaN-on-Si substrates :

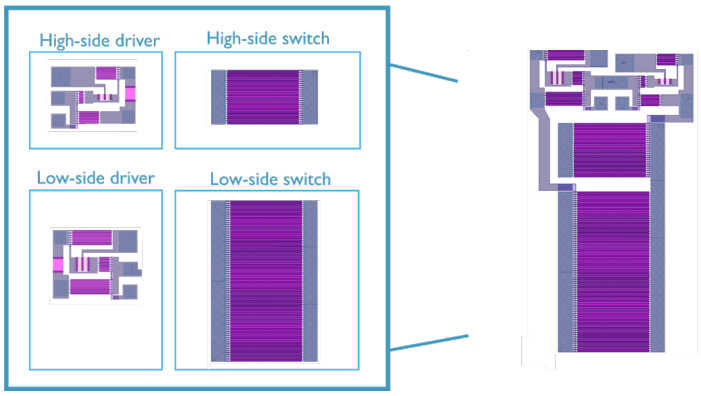
- The common Si substrate results in back-gating effects on the high-side power devices.
- The buried oxide of the SOI, the oxide-filled deep trenches and the deep Si contact effectively eliminate the back-gating effect.



Schematic cross-section of monolithically integrated half-bridge with enhancement mode low-side and high-side devices fabricated on 200 mm GaN-on-SOI with trench isolation.

DISCRETE COMPONENTS ON PCB

INTEGRATED HALF BRIDGE AND DRIVER



Monolithic integration of half-bridge and gate driver on imec's GaN IC platform.

To use the full potential of the fast switching speed of GaN power devices, the drivers should be co-integrated to lower the parasitic inductance.

Further functionality can be added through the low-voltage logic and analog switches, the high-ohmic and low-ohmic resistors and the integrated MIM-capacitors.

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