# A Complementary Dynamic Residue Amplifier for a 67 dB SNDR 1.36 mW 170 MS/s Pipelined SAR ADC

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***Abstract*— A complementary dynamic single-stage residue amplifier for a pipelined SAR ADC is presented. It re-uses charge typically wasted during the reset phase, and hence improves efficiency by a factor 2x in this block that often dominates the fundamental noise/power trade-off of the ADC. The residue amplifier achieves 90 µVrms input noise for an energy consumption of 1.5 pJ. It is used in a 2-times interleaved 6b coarse/8b fine pipelined SAR ADC. The 40nm CMOS prototype achieves 11 ENOB at 20 MS/s while consuming 165 µW, leading to an energy per conversion step of 4 fJ. It maintains more than 10.8 ENOB at low input frequencies for a clock frequency up to 180 MS/s.**

***Keywords*— *Pipelined SAR ADC, dynamic residue amplifier, Common mode detector, CMOS 40cm, SDR.***

## I. INTRODUCTION

Recent pipelined SAR ADCs leveraging dynamic residue amplification have achieved excellent performance at low power [1][2], combining most of the power efficiency of a SAR ADC and some of the speed of a pipeline ADC. One critical bottleneck in this architecture is the low noise and low power residue amplification. In [1], for example, the SNR is limited by thermal noise of the residue amplifier, which implies a 4x power penalty for 6 dB increase in SNR. In this paper, we present a more power efficient amplifier which achieves 6 dB lower noise for the same power, and thus allows one extra ENOB for the ADC with less than 20% power increase compared to [1].

## II. EFFICIENT DYNAMIC AMPLIFIER FOR HIGH RESOLUTION ADCS

Recently, several dynamic amplifiers have been proposed to replace the power hungry opamps in pipeline ADCs. These dynamic amplifiers use transconductors to convert the residue voltage to current which is integrated during a window of time on load capacitors. In the amplifier of Fig. 1a [3], both output voltages are initially reset to $V_{dd}$. During the amplification phase, a differential pair discharges two output nodes from $V_{dd}$ until a certain output common-mode voltage $V_{CM}$ is reached. At this point a common-mode detector switches off the input pair, freezing the output voltage. Assuming a certain $g_m/I_d$ biasing for the input pair during this amplification phase, the gain, noise and energy consumption can be approximated by expressions listed in Table 1. The amplifier shown in Fig. 1b [2] improves on this amplifier by using a cascode with some intermediate capacitance. As shown in Table 1, this technique can be used to increase the gain, but it has the same input-referred noise and energy consumption, and hence efficiency. The amplifier of Fig. 1c [1] uses a second stage rather than a common-mode detector to define the end of integration, but this second stage adds fairly significant differential noise while also consuming additional energy, as calculated in greater detail in [4] and shown in simplified form in Table 1.

Fig. 2 shows the complementary single-stage dynamic amplifier proposed in this work. In a first charging phase, the PMOS input pair determines the charging speed of nodes Out+/- while the NMOS input pair is disabled. After a certain time $T_{up}$ the PMOS devices are disabled and the NMOS pair is enabled. During this discharging phase the input is further amplified by the NMOS input pair. All the common-mode charge that was used during the charging phase is thus re-used to perform a further amplification of the input voltage. Once the output reaches a certain common-mode, as detected by a common mode detector (CMD), the discharging phase stops, similar to [3]. When the amplified output has been quantized, the differential nodes are not reset to ground or supply but only differentially, keeping the common-mode charge for the next amplification cycle.

Power consumption, input-referred noise and energy consumption can be approximated as listed in Table 1. Similar to complementary input opamps, the complementary input of this amplifier allows higher transconductance for a given current, and thus improves power efficiency, as defined by the product of input referred noise power and energy, by roughly a factor two compared to [2][3], and significantly more than a factor two compared to [1][4].

In our implementation a tunable delay line is used to control the charging time, and hence also the amplifier's gain. It is based on inverters driving a binary-scaled capacitor load allowing to control the pulse width of the signal used to charge the amplifier's output capacitors from 120 ps to roughly 600 ps.

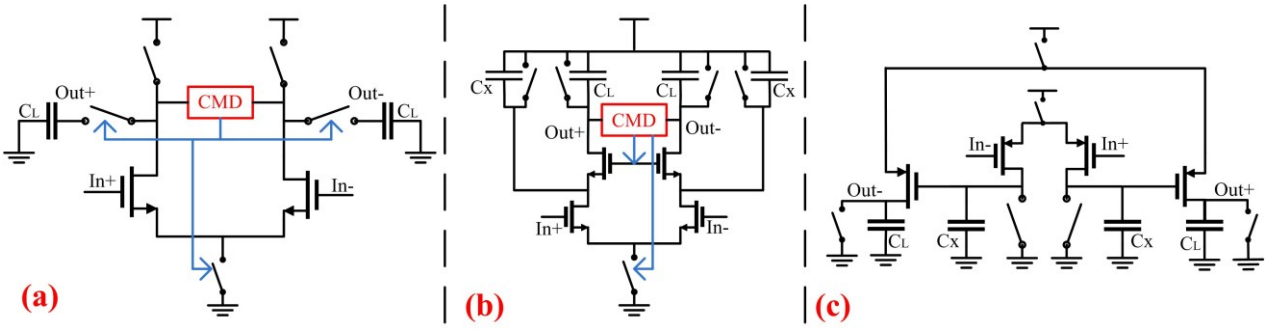


Figure 1: Schematics of different dynamic amplifiers

Table 1: Performance comparison for different dynamic amplifiers

| | Gain [-] | Input referred noise [$V^2$] | Energy [J] | Efficiency [$JV^2$] |
|---|---|---|---|---|
| **Single stage [3] Fig. 1.a** | $\frac{g_m \cdot (V_{dd} - V_{CM})}{I_D}$ | $\frac{4 \cdot k \cdot T \cdot \gamma}{g_m \cdot T_{int}}$ | $2 \cdot V_{dd} \cdot I_D \cdot T_{int}$ | $\frac{8 \cdot k \cdot T \cdot \gamma \cdot V_{dd}}{\frac{g_m}{I_D}}$ |
| **Cascode single-stage [2] Fig. 1.b** | $\frac{g_m \cdot (V_{dd} - V_{CM}) \cdot \left(1 + \frac{C_X}{C_L}\right)}{I_D}$ | $\frac{4 \cdot k \cdot T \cdot \gamma}{g_m \cdot T_{int}}$ | $2 \cdot V_{dd} \cdot I_D \cdot T_{int}$ | $\frac{8 \cdot k \cdot T \cdot \gamma \cdot V_{dd}}{\frac{g_m}{I_D}}$ |
| **Two-stage [1][4] Fig. 1.c** | $\frac{g_{m,in} \cdot g_{m,out,avg} \cdot T_{int}^2}{3 \cdot C_X \cdot C_L}$ | $\frac{4 \cdot k \cdot T \cdot \gamma}{g_m \cdot T_{int}} + v_{n,S2}^2$ | $2 \cdot V_{dd} \cdot I_D \cdot T_{int} + E_{Stage2}$ | $\frac{8 \cdot k \cdot T \cdot \gamma \cdot V_{dd}}{\frac{g_m}{I_D}} + X$ |
| **Complementary single-stage [proposed] Fig. 2** | $\frac{T_{up} \cdot \left(g_{mP} + g_{mN} \cdot \frac{I_{DP}}{I_{DN}}\right)}{C_L}$ | $\frac{4 \cdot k \cdot T \cdot \gamma}{\left(g_{mP} + g_{mN} \cdot \frac{I_{DP}}{I_{DN}}\right) \cdot T_{up}}$ | $2 \cdot V_{dd} \cdot I_{DP} \cdot T_{up}$ | $\frac{8 \cdot k \cdot T \cdot \gamma \cdot V_{dd}}{\left(\frac{g_{mP}}{I_{DP}} + \frac{g_{mN}}{I_{DN}}\right)}$ |

The CMD used to end this discharging phase is implemented using two capacitors of 100 fF each to sense the output common-mode which is then followed by the inverter-like circuit shown in Fig. 3.

When the amplifier is in the charging phase, the CMD output is pulled to ground. During the discharging phase, the CMD output starts charging and when the output reaches a certain level, the following inverter is triggered, which stops the amplifier discharging and disconnects the load capacitor from the amplifier.

In this two-phase implementation, the rising common-mode during the charging phase limits $T_{up}$ and thus the gain. Higher gains are possible by alternating charging and discharging phases, ultimately limited only by output impedance $g_{ds}$ and distortion. In our prototype ADC, a voltage gain of roughly 4 is sufficient, which can easily be achieved in two phases. The charging and discharging phases could also be done simultaneously, but this requires large common-mode feedback devices that add significant parasitics at the amplifier's output [5]. To linearize the input capacitance of the amplifier, the input devices are biased in depletion mode when the amplifier is not used using additional switches not shown in Fig. 2.

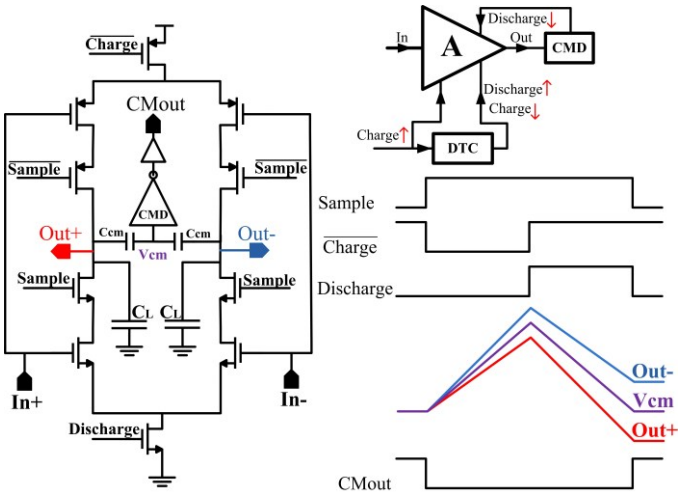


Figure 2: Complementary dynamic amplifier and its waveforms

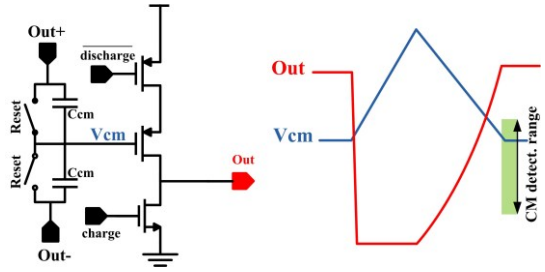


Figure 3: the CMD and its waveforms

## III. ADC PROTYTYPE

The proposed amplifier is implemented in a prototype ADC intended for use in a wireless receiver. The latest wireless standards impose stringent requirements for linearity and speed of data converters. In addition, increasing the ADC sampling rate or resolution reduces the required channel filtering and allows for a simpler and faster AGC. Since most of the target applications are portable, the ADC power efficiency is also critical. The ADC architecture (Fig. 4) uses two interleaved channels, each of which uses a 6b coarse SAR, the dynamic residue amplifier and an 8b fine SAR. In the default mode, the converter implements 12b for quantization and has a total of 2b for redundancy.

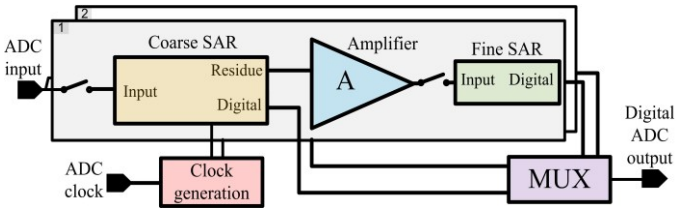


Figure 4: Architecture of the ADC

The channel implementation is shown in Fig. 5: an interleaved bootstrapped sampling switch is used to sample the input signal on the DAC of the coarse SAR during a tracking time of half the conversion rate period. To obtain simulated 12b DAC matching with 99.85% yield, a 2 pF DAC array with 0.34 fF step MSB calibration is used. Furthermore, to reduce inter-channel gain errors, the range of this coarse stage DAC is also calibrated, in a range of approximately ±1.3% with a step of 0.02%.

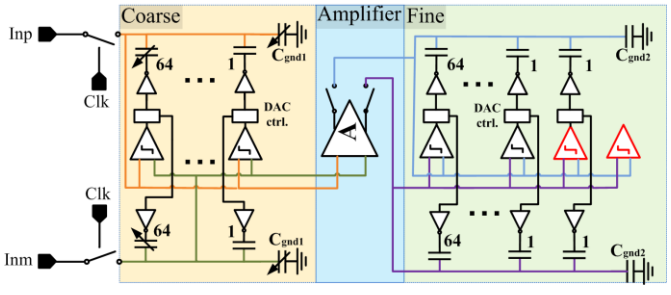


Figure 5: Detailed implementation of the ADC

Since the dynamic amplifier requires a common-mode input around mid-supply voltage, the DAC has a first step-down MSB feedback and step-up operation for the other five bits. As in [1], 6 comparators are used to digitize each bit asynchronously, avoiding the use of a SAR controller and also allowing each comparator offset to be calibrated with an accurate common-mode input level. The second stage has a step-down feedback DAC, 6 fast and high noise comparators, and 2 slow and low noise comparators used for the last 2 bits. All comparators are implemented using the topology of [6] with offset calibrated by digitally controllable capacitors. The DAC unit capacitance in the fine SAR stage is around 1 fF. A capacitor to ground is added to limit the DAC range, for a total amplifier load capacitance of around 380 fF excluding the CMD sensing capacitor.

In the nominal mode, where 12b quantization noise level is targeted, the amplifier gain is approximately 3.6 to allow a factor 2 of redundancy between the coarse and fine stages as in [1]. According to simulations, this amplification takes 1.2 ns and generates roughly 90 µV input referred RMS noise, while consuming less than 1.5 pJ. Compared to [1], amplifier noise is reduced by a factor two without a power penalty. The amplifier achieves 63 dB THD with a 40mVpp differential input, which does not impact the 7b effective fine SAR.

## IV. MEASUREMENTS

A die micrograph is shown in Fig. 6, the prototype is manufactured in 1.1 V 1P7M 40 nm low-power CMOS technology in a core area of 180 µm×380 µm.

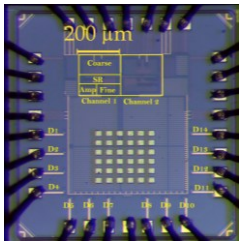


Figure 6: Die micrograph

Comparator offsets, amplifier gain and MSB capacitance are calibrated offline and off-chip using a shorted input as in [1]; channel gain and time skew are also calibrated, which can be done in the background with fairly arbitrary inputs [7]. The DNL and INL at 20 MS/s are within -0.58/0.45 LSB and -1/0.89 LSB respectively as shown in Fig. 7.

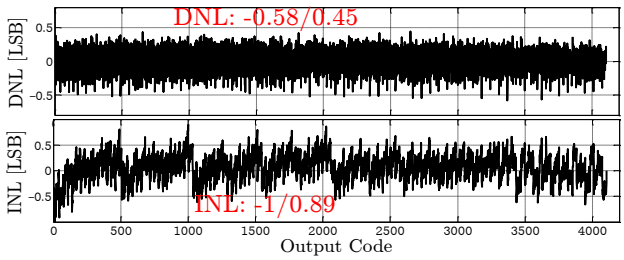


Figure 7: DNL/INL @ 20 MS/s

With an approximately 10 MHz input signal, the ADC achieves 11 ENOB at 20 MS/s and 10.88 ENOB at 170 MS/s as shown in Fig. 8.

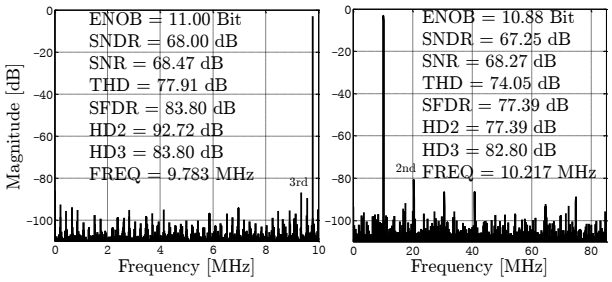


Figure 8: FFT @ 20 MS/s and 170 MS/s

Fig. 9 shows the SNDR/SFDR vs. input frequency for 20 MS/s, 170 MS/s and 200 MS/s. High frequency SNDR is limited by 3rd order and mismatch spurs as well as jitter.

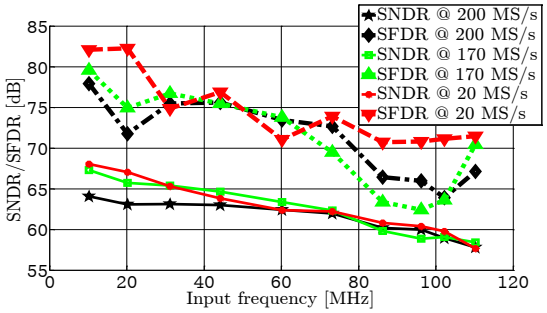


Figure 9: SNDR/SFDR @ 20 MS/s, 170MS/s and 200MS/s

The ENOB vs. clock frequency is shown in Fig. 10, ranging from 11 ENOB at low clock and input frequencies to 9.6 ENOB at 200 MS/s with Nyquist input. Since the ADC consumes 8.25 pJ, the energy per conversion step is between 4 fJ and 10 fJ as shown in Fig. 10.

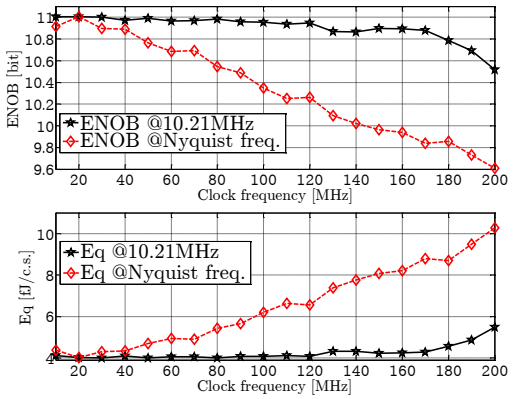


Figure 10: ENOB and FoM of the ADC @ 10 MHz input and Nyquist

To explore the limits of the amplifier noise and since the amplifier is robust to distortion and not all of the 2x coarse/fine redundancy is needed if calibration is accurate, a higher amplifier gain can also be used when clock speed is not critical. For instance, if the amplifier gain is increased to implement 12.6b quantization noise, the ADC consumes 170µW and achieves 70 dB SNDR with a Nyquist input at 20 MS/s, corresponding to 3.25 fJ/c.s.. In this mode, the Schreier FoM is 177.8 dB. Fig. 11 shows the Schreier FoM at 20 Ms/s and 170 MS/s compared to state of the art [8].

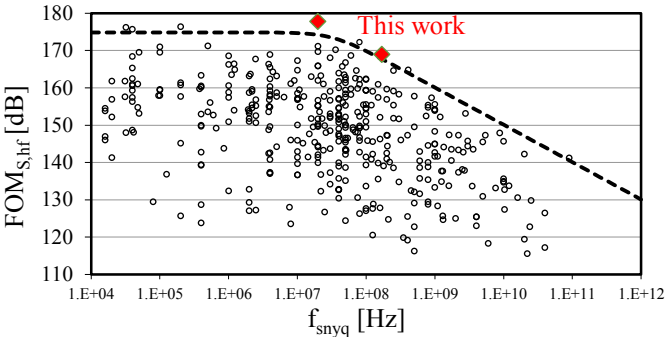


Figure 11: State of the art comparison

## V. Conclusion

A complementary dynamic amplifier is shown to reduce noise power by a factor 2 with no impact on power consumption compared to existing dynamic amplifiers. This allows a 6 dB improvement in the SNDR of a pipelined SAR ADC with less than 20% energy increase compared to [1], leading to an attractive solution for multi-standard wireless receivers.

## VI. Acknowledgments

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