

A 70 dB SNDR 200 MS/s 2.3 mW dynamic pipelined SAR ADC in 28nm digital CMOS

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Abstract

We present a 200 MS/s 2x interleaved 14 bit pipelined SAR ADC in 28nm digital CMOS. The ADC uses a new residue amplifier for low noise at low power, and incorporates interleaved channel time-constant calibration. The ADC achieves a peak SNDR of 70.7 dB at 200 MS/s while consuming 2.3 mW from an 0.9 V supply.

Motivation

In a software defined radio, the ADC needs a speed of at least 200 MS/s and as much resolution as is feasible for a power budget of a few milliwatts, in order to simplify AGC and relax filtering requirements. In addition, since this ADC also needs to quantize much lower bandwidth standards, a dynamic solution is desirable. For these requirements, the pipelined SAR architecture [1] is the most likely candidate. However, the two-stage residue amplifier in [1] limits SNR to approximately 64 dB, whereas this design uses a more efficient single-stage complementary residue amplifier. In addition, this design adds calibration to reduce spurs from DAC non-linearity and channel time-constant mismatch. These improvements result in up to 10 dB increased SNDR with less than 2x energy increase compared to [1], which results in a peak Schreier FoM of 177.4 dB at 20 MS/s.

Architecture and channel implementation

The ADC architecture consists of two identical channels, each of which comprises a 6b coarse SAR, a complementary dynamic residue amplifier and a 10b fine SAR, as shown in Fig 1. Two 1b redundancies, between coarse and fine SAR and between the first 8 and last 2 cycles of the fine SAR respectively, result in 14b quantization. A front-end sampling switch eliminates time skew, while channel gain and time-constant are calibrated digitally as explained later.

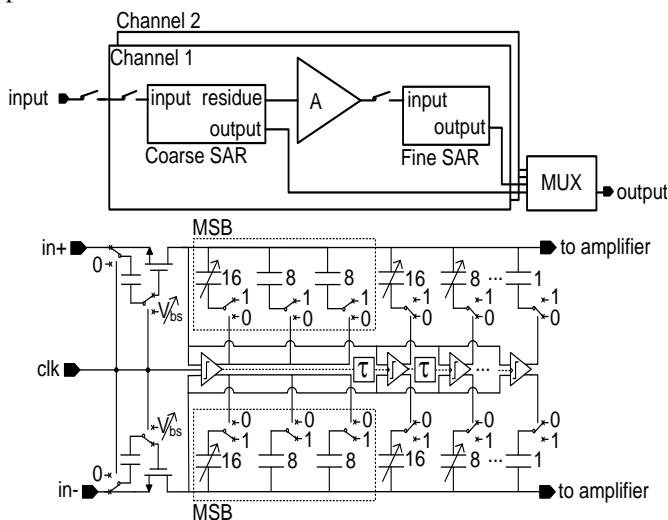


Figure 1: Block diagram of ADC (top) and simplified coarse SAR schematic (bottom).

Both coarse and fine SAR are comparator-controlled [2] to eliminate the need for a SAR controller by using 6 and 10 different comparators in coarse and fine stages respectively. These are arranged to directly generate DAC feedback and asynchronously clock the next comparator in line as illustrated in Fig. 1. Both DACs use single-ended switching, but while in the fine stage the

DAC uses step-down switching [2] exclusively, in the coarse stage the MSB switches down while LSBs switch up, to result in approximately the same common-mode for residue voltage and ADC input voltage, which allows the use of the complementary residue amplifier explained below. The channel gain is tuned using a programmable parasitic capacitor at the top plate of the coarse SAR as in [1].

The single-ended coarse DAC arrays are chosen 3.5 pF for 13b KT/C noise. To ensure sufficient matching the three MSB weights are calibrated. This automatic calibration uses the fine SAR to measure amplified capacitor mismatch that is generated by the coarse SAR. Since the second stage is sensitive to common-mode input, this calibration step requires the ability to generate a differential signal proportional to the capacitor mismatch with the appropriate common-mode value, which is not straightforward in a single-ended switching scheme. In this design, the MSB capacitor is split into one half-size and two quarter-size segments as shown in Fig. 1 (bottom). By directly controlling all DAC capacitors (not shown in Fig. 1), these segments can thus be switched down to compensate for the common-mode shift due to switching up of MSB-1 and MSB-2 during their calibration. During normal operation all three MSB capacitor segments are switched together.

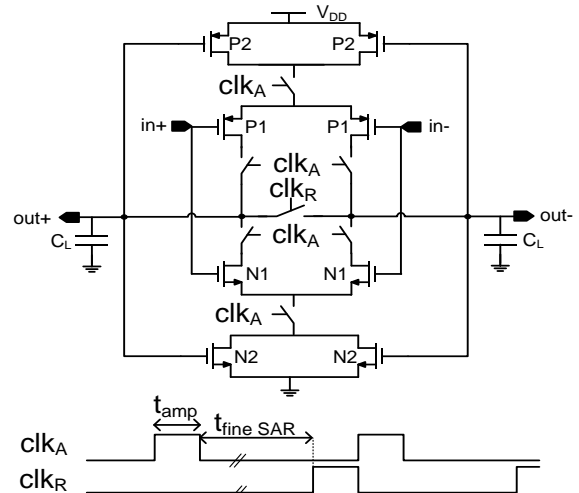


Figure 2: Simplified schematic of complementary residue amplifier with clock waveforms.

A key enabler in lowering the thermal noise floor of the ADC without a detrimental impact on power consumption is the complementary residue amplifier shown in Fig. 2. During amplification, switches controlled by clk_A are closed and transistors N1 and P1 generate an output current difference which is integrated on a 3.5pF single-ended load capacitance, which includes the 0.5 pF fine SAR DAC. After a certain time t_{amp} , the clk_A switches open, turning off the current flow in the amplifier and fixing the output voltage, which can then be quantized by the fine SAR. When the fine SAR quantization is finished, the switch controlled by clk_R is closed, which shorts the differential outputs. The amplifier common-mode gain is reduced by the N2 and P2 devices. The delay line controlling t_{amp} is designed to track changes in g_m in first order, which stabilizes voltage gain to a large

degree across corners. Digital delay control is used to fine-tune the voltage gain during a foreground or background calibration as in [1]. By reducing the number of relevant noise sources to just N1 and P1, and biasing these using the same current, this simple amplifier combines low power and low noise. As no charge is lost in resetting the outputs to ground, all supply current is used optimally for amplification. In typical conditions an input referred noise of $40 \mu\text{V}$ r.m.s. i.e. is achieved for an energy consumption of approximately 2.3 pJ . In addition, since the amplifier does not rely on closed-loop settling it can be designed for high speed: the target voltage gain of 4 is achieved after only 630 ps .

Channel time-constant calibration

In interleaved converters, channel time-constant mismatch can seriously degrade high-frequency accuracy [3]. This effect occurs due to mismatch in the on-resistance of the channel sampling switch or sampling capacitor, and causes amplitude and phase errors at high input frequencies. Designing this sampling network for intrinsic matching is complicated by the fact that the sampling capacitors are not necessarily located in close proximity in layout, which means typical foundry matching data is unreliable. In this design we thus choose to avoid this potential issue by adjusting the channel time-constant using a programmable bootstrap voltage V_{bs} for the channel sampling switches, as shown in Fig. 1.

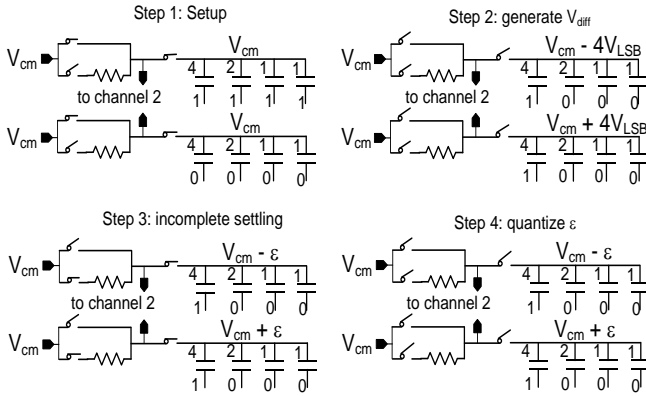


Fig. 3: Four steps in shorted input settling error detection.

Channel time-constant mismatch is detected in an automated shorted-input calibration using the scheme illustrated in Fig. 3. First, the ADC input common-mode is sampled on the coarse DAC array, with its bottom plates pre-charged to an imbalanced state. In the second step, the DAC array is switched to its default initial condition, which generates a voltage difference. In the third step, the DAC top plates are connected to a zero differential input through a redundant front-end switch with some explicit resistance in series. This creates a settling error on the DAC top plates which can then be quantized by normal ADC operation and compared between channels in step 4. The quantized difference can then be used to estimate a difference in settling error and thus to estimate time-constant mismatch. This calibration step thus only requires simple digital operations and a shorted ADC input, avoiding high frequency calibration signals and complex signal processing.

Measurement results

The ADC prototype has been manufactured in a 1P9M digital 28nm HPM CMOS process and occupies 0.35 mm^2 including 1 nF of reference decoupling capacitance (Fig. 4). This reference is shared by both channels and also acts as a supply: all power is drawn from this reference. A shorted-input foreground calibration corrects for comparator offset, capacitor mismatch, residue amplifier gain, channel gain and finally channel time-constant, in this order. In this prototype all calibration is controlled from Matlab on a PC, but it could be integrated on-chip as in [1].

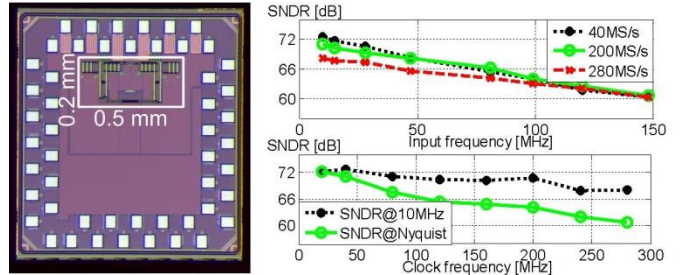


Fig. 4: Chip micrograph (left), SNDR vs. input frequency (top right) and SNDR vs. clock frequency (bottom right).

As shown in Fig. 4, the prototype achieves a peak SNDR of 72.7 dB at 40 MS/s with a 10 MHz input, with INL and DNL within approximately $\pm 2 \text{ LSB}$ which is acceptable considering the 14b quantization noise and approximately 12b target resolution. Low-frequency SNDR is above 70 dB up to 200 MS/s and more than 68 dB up to 280 MS/s . High frequency behavior is in part degraded by jitter from the measurement setup: SNDR degrades to just over 60 dB at 150 MHz input, regardless of clock frequency.

The effectiveness of the time-constant calibration is illustrated in Fig. 5, which shows the magnitude of the skew spur at $F_{\text{clk}}/2 - F_{\text{in}}$ and settling error difference (bottom) vs. time-constant calibration code. As expected, the zero-crossing of the settling error difference corresponds closely to the optimum spur performance.

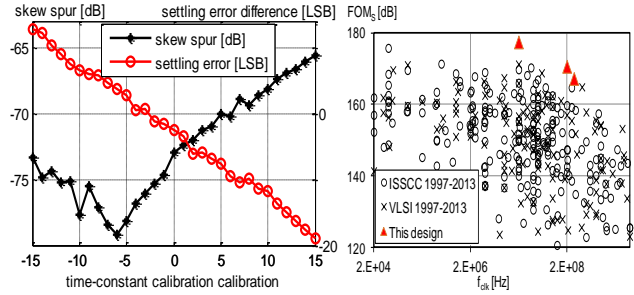


Fig. 5: Skew spur measured at 200 MS/s with 95 MHz input and settling error difference (left) and state of the art comparison [4] (right).

The ADC consumes approximately $90 \mu\text{A}$ of leakage and $11 \text{ pJ}/\text{conversion}$ dynamic energy from the 0.9 V reference, resulting in energy per conversion step between $3.7 \text{ fJ}/\text{conv. step}$ at 40 MS/s with a low frequency input, and $12.8 \text{ fJ}/\text{conv. step}$ at 280 MS/s with a Nyquist input, despite limitations in the measurement setup. Schreier FOM is 177.4 dB at 20 MS/s , 170.6 dB at 200 MS/s and 167.2 dB at 280 MS/s which compares favorably to state of the art as shown in Fig. 5. In addition, due to low additive noise, this design offers excellent dynamic range for its power consumption, making it a good candidate for SDR receivers.

References

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