27.5 A 1.7mW 11b 250MS/s 2× Interleaved Fully Dynamic Pipelined SAR ADC in 40nm Digital CMOS

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In recent years ADC research has resulted in impressive advances in power efficiency. SAR ADCs have reached energies per conversion step below 10fJ, but only at rather low sampling frequencies [1] or moderate resolution [2]. Wireless receivers for next-generation, higher-bandwidth standards such as LTE-advanced, however, will require much faster ADCs. We present a fully dynamic, two-times interleaved pipelined SAR ADC that achieves 10fJ/conversion-step with 9.5 ENOB at a sampling speed as high as 250MS/s.

Figure 27.5.1 shows a block diagram of the ADC, consisting of a bootstrapped front-end sampling switch operating at the full clock frequency, two interleaved ADC channels and a multiplexer combining their outputs. The front-end sampling switch uses a 50% duty cycle and turns off first, eliminating potential timing mismatch between the two channels. Each channel consists of a 6b coarse SAR ADC, a dynamic residue amplifier with a sampling switch at its output and a 7b fine SAR ADC to quantize this residue. Since two factor 2 redundancies are implemented, the converter has 11b quantization noise.

Figure 27.5.2a shows the coarse SAR ADC implementation. As in [2] it uses a step-down DAC and the comparators themselves implementing the controller: each cycle of the SAR ADC has its own dynamic comparator, clocked in sequence by the preceding comparator with an appropriate delay to allow for DAC settling. The comparators are based on [3] with their offsets calibrated off-line using digitally controllable capacitance. Since each comparator is only clocked in a specific cycle the changing common-mode of the chosen DAC [4] is not an issue. In the coarse SAR, a series sampling capacitance (C_s) of 1pF is used, reducing the input capacitance compared to the 2pF DAC. The bottom plate of this sampling capacitance is tied to V_{DD} during sampling, and then discharged by the DAC during the SAR algorithm. To correct for DAC capacitor mismatch and inter-channel gain errors, digital calibration is added for the MSB capacitance and top-plate DAC capacitance, respectively. After the coarse SAR has finished, the residue of this conversion is conveniently available at its comparator inputs.

The amplification of this residue is implemented using the dynamic amplifier of [5] as shown in Fig. 27.5.3. During the coarse SAR operation the amplifier clock is high and the amplifier is reset. The sample and reset signals controlling the fine SAR are asynchronously brought high when the fine SAR is ready to receive the next amplified residue or when the coarse SAR is nearly done, whichever occurs first in a given clock cycle. When the first stage has generated its residue, the reset signal and amplifier clock are brought low, and nodes D+ and D- are charged from ground up to V_{DD} with speeds depending on the in+ and in- voltages. During this charging, current flows through the P3, P2 and sampling transistors into the fine SAR DAC capacitance (C_{DAC2}), building up a voltage on these nodes. When the D+ and D- nodes reach V_{DD} the P2 transistors turn off, stopping all current flow in the amplifier and freezing the amplifier output voltage. The sampling signal is then brought low, disconnecting the fine SAR from the amplifier. Finally, the amplifier is reset and the coarse SAR can start processing the next sample while the fine SAR starts quantizing the sampled residue, i.e. both stages are pipelined.

The P3 transistors in Fig. 27.5.3 implement common-mode feed-forward path, reducing the common-mode gain of the amplifier. When the input common-mode increases, D+ and D- are charged more slowly and the P2 transistors are on for a longer time, resulting in higher common-mode output voltage. The P3 transistors counter this trend by decreasing the current through the P2 transistors. The amplifier gain is controlled with a 7b gain-control unit. By leaving the bottom plate of the 2.5fF capacitance units floating during the critical charging of D+ and D- rather than permanently connecting it to ground, the slope of D+ and D- can be increased, thus decreasing the amplifier gain. To guarantee sufficient (>6b) linearity the amplifier output range is kept limited to roughly $100mV_{pp}$ differential with a voltage gain of approximately 4. During an offline calibration, the amplifier gain is tuned such that 1 LSB of the coarse stage corresponds to 1 MSB of the fine stage. Since the total range of the second stage is then two first-stage LSBs, this results in a factor 2 redundancy, which can correct for settling errors in the first stage. By matching the bit weights of the two stages their outputs can be combined using a simple shift and add operation, without digital multipliers.

Figure 27.5.2b shows the implementation of the fine SAR, using a step-down DAC directly controlled by comparators as in the coarse SAR. However, since the DAC capacitance required for sufficient matching is very small, no series sampling capacitance is used. Rather, a fixed capacitance to ground (C_1) is added to reduce the DAC range and lower the sampled noise. The total size of the fine SAR DAC capacitance is 62fF, limited by the size of a unit capacitance, while C_1 is roughly 600fF. To compensate for errors due to comparator noise the 5th and 6th comparison generate the same weight feedback for a factor 2 redundancy between these decisions. Similar to [6] the 6th and 7th comparators are implemented with lower noise and speed, as shown in bold in Fig. 27.5.2b.

The ADC is manufactured in a 1P7M 40nm low-power CMOS process with a core chip area of $0.066mm^2$ (Fig. 27.5.7). A 3-step, shorted input off-line calibration procedure is used to tune comparator offset, residue amplifier gain and the MSB capacitance size in the coarse SAR, in that order. A zero differential input signal at the ADC common-mode is transformed into a zero signal of the correct common-mode at the input of a comparator by directly controlling the internal DACs, and comparator offset is calibrated by observing its average output. This is repeated 13 times for all comparators in the ADC. Next, the same zero input is transformed into a ±0.5 LSB differential signal by direct control of the coarse DAC, and the amplifier gain is calibrated by measuring its output using the second stage. In a third step, the MSB capacitance (so far not used by DAC control) mismatch is measured using the now-calibrated amplifier and second stage. Finally, gain and offset errors between the two channels are measured by applying some non-zero inputs and observing both channels. Gain mismatch is calibrated by changing the top-plate DAC capacitance in the coarse stage, offset is corrected digitally. For full flexibility in this prototype, calibration is controlled by Matlab on a PC, but the controller could easily be integrated in VHDL.

At 10MS/s the DNL for each channel is within -0.75/+1LSB, and the INL is within -1.75/+1.25LSB as shown in Fig. 27.5.4. Due to averaging, the overall DNL and INL are improved to -0.5/+0.8LSB and -1.5/+1.1LSB respectively. Fig. 27.5.5 (top) shows the SNDR and SFDR vs. input frequency at 10 and 250MS/s. At low sampling and input frequencies the SNDR is 62dB, increasing the sampling frequency to 250MS/s degrades this to 58.7dB. At this clock frequency, the SNDR remains above 56dB up to the Nyquist frequency. Figure 27.5.5 (bottom) shows a spectrum of the ADC output with an 11MHz input sampled at 250MS/s. The calibrated gain mismatch spur near 114MHz is below -70dBFS, and does not affect the SNDR.

The ENOB versus clock frequency for two input frequencies is shown in Fig. 27.5.6 (top). Since the ADC consumes 6.9pJ/conversion from a 1.1V supply the total power consumption is 70µW at 10MS/s and 1.7mW at 250MS/s. From 10 to 250MS/s, the energy per conversion step is between 7 and 10fJ for low-frequency inputs and between 7 and 13 fJ for near-Nyquist inputs. This shows the potential of the ADC for low-power LTE-advanced receivers.

References:

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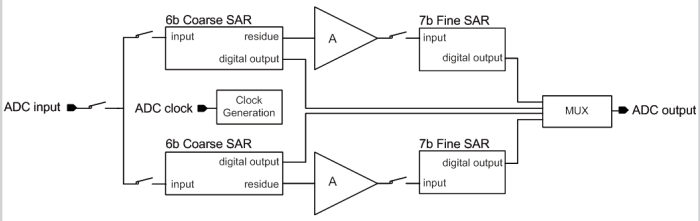

Figure 27.5.1: Block diagram of the implemented ADC.

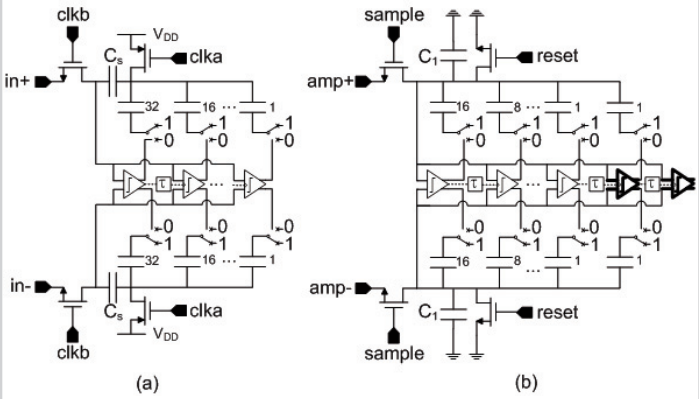

Figure 27.5.2: Simplified architecture of the coarse SAR stage (a) and the fine SAR stage (b).

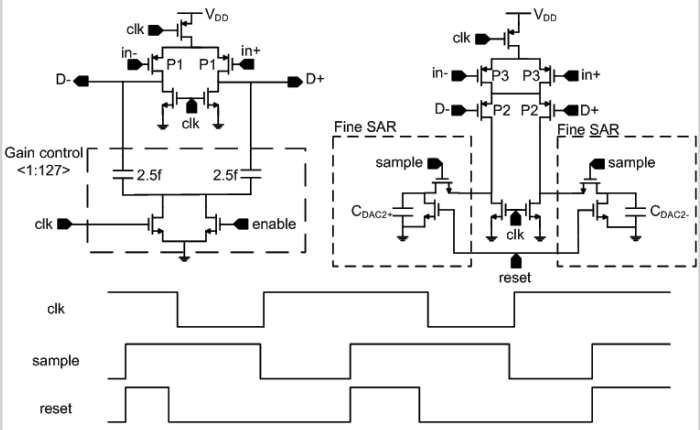

Figure 27.5.3: Schematic of the dynamic residue amplifier and clock waveforms for this amplifier and the fine SAR.

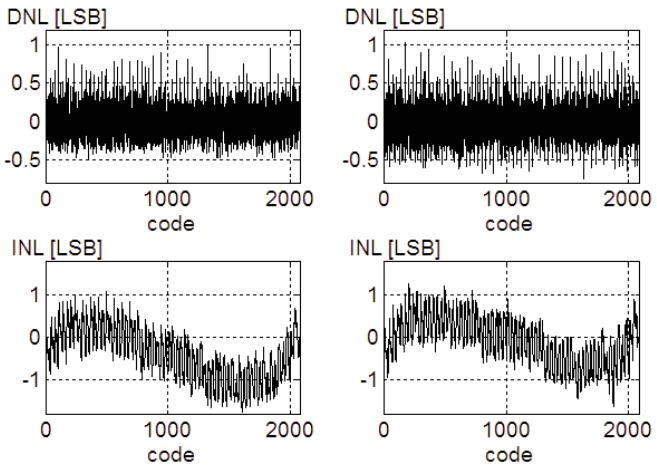

Figure 27.5.4: DNL (top) and INL (bottom) of channel 1 (left) and channel 2 (right) of the ADC.

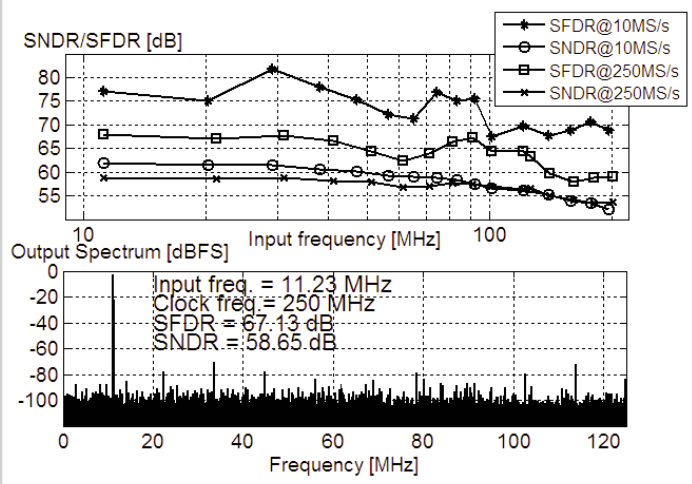

Figure 27.5.5: SNDR/SFDR vs. input frequency at 10MS/s and 250MS/s sampling frequency (top) and measured output spectrum at 250MS/s (bottom).

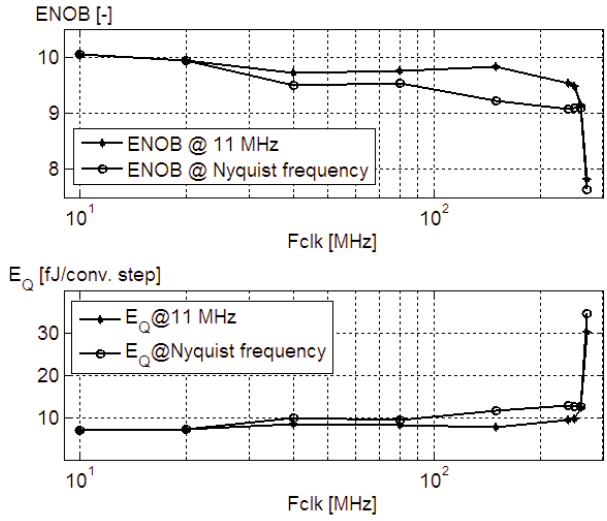

Figure 27.5.6: Measured SNDR and SFDR (top) and energy per conversion step (bottom) as a function of clock frequency.

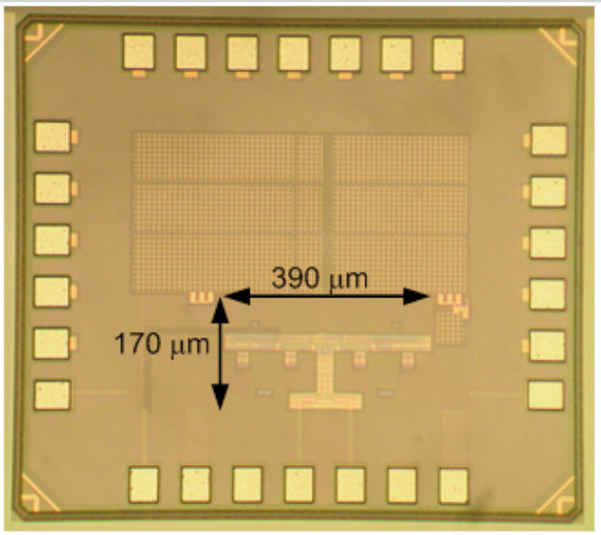

Figure 27.5.7: Chip micrograph with core size indicated.

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