A 2.1 mW 11b 410 MS/s Dynamic Pipelined SAR ADC with Background Calibration in 28nm Digital CMOS

Bob Verbruggen[1], Masao Iriguchi[2], Manuel de la Guia Solaz[1], Guy Glorieux[1], Kazuaki Deguchi[2], Badr Malki[1,3], Jan Craninckx[1]

[1]imec, Kapeldreef 75, Leuven, Belgium   [2]Renesas Electronics, Japan   [3]Vrije Universiteit Brussel, Brussels, Belgium
Email: bob.verbruggen@imec.be

Abstract

A 410 MS/s 2x interleaved 11bit pipelined SAR ADC in 28nm digital CMOS is presented. Each ADC channel consists of a 6b coarse SAR, a dynamic residue amplifier and a 7b fine SAR and includes an on-chip calibration engine that detects and corrects comparator offsets and amplifier gain errors in the background. The ADC achieves a peak SNDR of 59.8 dB at 410 MS/s for an energy per conversion step of 6.5 fJ.
Keywords: pipelined SAR, calibration

Motivation and proposed approach

It has been shown that digital calibration can significantly improve ADC power efficiency for a wide range of resolutions and speeds [1,2,3]. As technology scales, the power and area cost of implementing said calibration decreases, while the analog impairments such as offsets or gain errors typically scale only slowly or not at all. In this work, we target a background calibrated ADC for LTE-advanced wireless receivers, using the dynamic pipelined SAR architecture of [4].
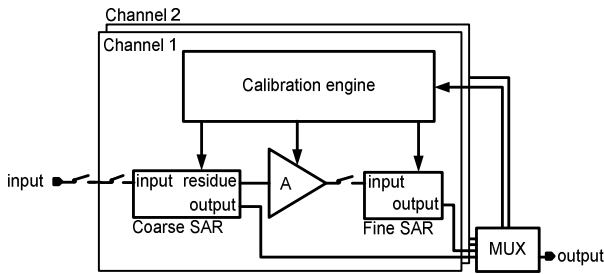

Fig. 1: ADC block diagram.

Fig. 1 shows a block diagram of the interleaved ADC. A bootstrapped front-end sampling switch operating at the full rate eliminates time skew between two identical ADC channels operating at half the clock rate and opposite phase; a multiplexer combines and synchronizes the outputs of the two channels. As in [4] each ADC channel consists of a 6b coarse SAR ADC, a dynamic residue amplifier with a sampling switch at its output and a 7b fine SAR ADC to quantize this residue. Two one bit redundancies are implemented: the first between coarse and fine SAR ADCs and the second between the first 5 and the last 2 cycles of the fine SAR. As in [4] both coarse and fine SAR ADCs use multiple comparators to implement the controller. While this avoids the power and speed overhead of a conventional SAR controller, this approach is sensitive to comparator offsets. Since each conversion uses 13 comparisons, each implemented by a different comparator, there are 13 comparator thresholds to be calibrated in each channel. In addition, since the implemented dynamic residue amplifier gain is quite sensitive to process and temperature changes, this gain also needs to be calibrated.

Calibration engine

The 6 coarse SAR and first 5 fine SAR comparator offsets are calibrated using the redundancy between coarse stage and fine stage and the redundancy between first 5 and last 2 fine stage comparators respectively, as illustrated in Fig. 2a). If the quantized residue exceeds its ideal residue range, an error has occurred. This error can be attributed to a certain comparator based on the comparison results before and after redundancy using simple combinatorial logic. The number of incorrect positive and negative decisions for each comparator is averaged and when the difference between the two types of error exceeds a programmable limit, the appropriate comparator threshold is adjusted. This averaging reduces the impact of noise and input statistics on the offset corrections.

The last two comparators of the fine SAR converter are calibrated using their output histogram. With ideal comparator thresholds a symmetric output histogram is obtained as shown in gray in Fig. 2b), which corresponds uniquely to a 50% distribution of each comparator output. The output histogram is accumulated during a programmable number of cycles and comparator thresholds are adjusted if less than 25% or more than 75% of decisions is positive. Both this loop and the comparator threshold calibration loops for the first 11 comparators are running simultaneously and converge easily to a steady state value.
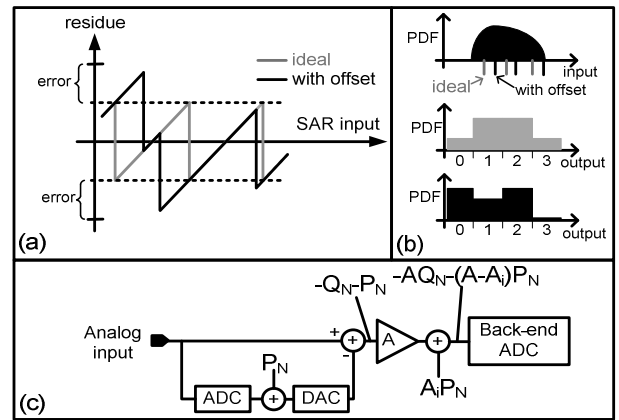

Fig. 2: Illustration of calibration algorithms.

The residue amplifier background calibration is done by adding a pseudo-random signal P_N to the residue amplifier input as in [5]. However, contrary to [5], a scaled version of this dither signal is subtracted at the output of the amplifier by the second stage DAC before the fine SAR quantization as shown in Fig. 2c). The residue gain error can still be estimated by correlating the fine SAR output with the pseudo-random sequence similar to [3,5]. However, since in the absence of residue gain error the dither signal only affects the residue

amplifier, the added dither does not affect the required input range of the fine SAR [5] or the first stage quantization error budget [3].

All the above calibration algorithms are implemented in VHDL along with a foreground calibration procedure slightly modified from [4] and a serial programming interface. To reduce the calibration engine dynamic power, its clock rate can be reduced by powers of 2 up to 1024 by a programmable clock divider. This allows a trade-off between the background calibration convergence speed and power consumption.
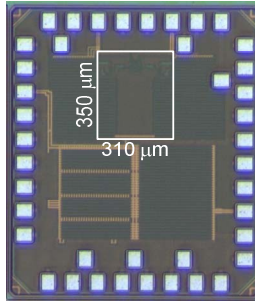

Fig. 3: Die micrograph with core area indicated.

Measurement results

The ADC prototype has been manufactured in an 1P9M 28nm CMOS process with a core chip area of 0.11 mm^2 which includes the calibration engines but not decoupling (Fig. 3). Gain and offset mismatch between the two channels are measured by applying non-zero inputs and observing both channel outputs. Gain mismatch is calibrated by changing the top plate DAC capacitance in the coarse SAR, offset is compensated digitally.

The behavior of the background calibration is measured by programming the chip in default settings and applying a full-scale sine wave input. The SNDR calculated in 16k windows with variable start point is shown in Fig. 4 for different divider ratios for the calibration engine clock: the background calibration converges within approximately 50k cycles per channel. Alternatively, an on-chip shorted input foreground calibration can provide correct settings in less than 3k cycles per channel. After this a slow background calibration is sufficient to track slow changes in the environment.
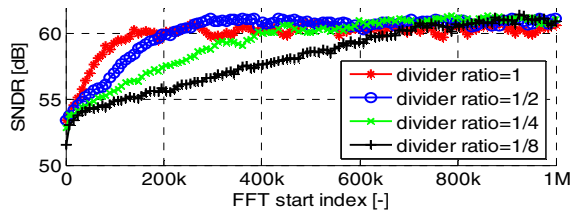

Fig. 4: SNDR vs. start index after programming defaults.

At 20 MS/s the DNL for each channel is within -0.6/1.2 LSB, and the INL is within -0.8/2.2 LSB as shown in Fig. 5. The INL is degraded by systematic mismatch in both channels and on different samples. This is due to unintended front-end dummies in the first stage DAC and is compensated by adjusting the first stage bit weights for the remaining measurements. Fig. 6 shows the SNDR vs. input frequency at different clock frequencies (top): at 20 MS/s the ERBW is limited by external clock phase noise, at higher clock

frequencies ERBW exceeds 130 MHz. A 136 MHz input sampled at 260 MS/s yields an SFDR of 68 dB as shown in the middle plot of Fig. 6. The bottom plot of Fig. 6 shows SNDR vs. clock frequency measured with slow background calibration. The low input frequency SNDR degrades from 62.5 dB at 10 MS/s to 59.8 dB at 410 MS/s. The circuit consumes 100 µA leakage current, 5 pJ per ADC clock cycle and 3.3 pJ per calibration engine clock cycle from a 0.9 V supply. Peak efficiency is 5.5 fJ/conv. step at 110 MS/s and less than 12 fJ at 410 MS/s with a Nyquist input signal, which includes power required for slow background calibration. This clearly demonstrates the viability of the proposed approach for a robust low-power receiver.
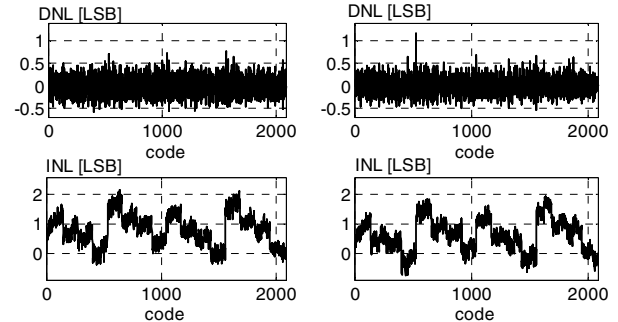

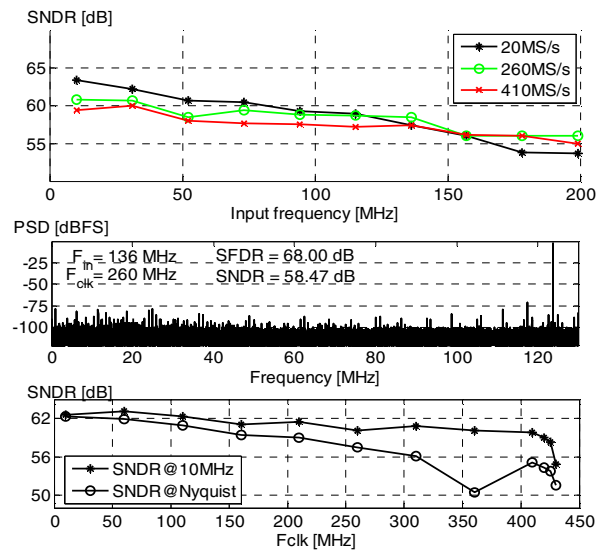Fig. 5: INL and DNL for individual channels.

Fig. 6: SNDR vs. input frequency (top), output spectrum (middle) and SNDR vs. clock frequency (bottom).

References

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