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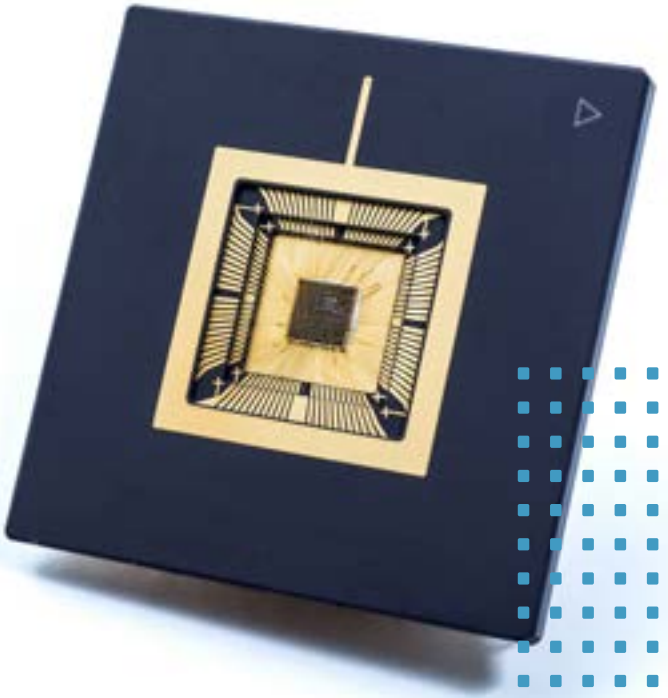

IMEC CONTRIBUTIONS AT IEDM 2019

TOWARDS NEXT-GENERATION COMPUTING

Location all sessions: Hilton San Francisco Union Square 333 O'Farrell Street San Francisco, CA 94102, USA

Imec will present
6 invited papers,
24 technical papers and
wil co-chair 4 sessions
at the IEDM 2019
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MONDAY, DECEMBER 9

> Imec's well-equipped labs for processing, characterization and design enable me to execute experiments quickly. Any problem – whether it is software or hardware-related – is swiftly dealt with by imec's professional support teams. As I can easily approach any of imec's world-class semiconductor experts, working on my PhD here provides me with a much wider viewpoint than most of my peers have.

_Xiangdong Li

SESSION 4

POWER DEVICES AND SYSTEMS - ADVANCES IN GAN POWER DEVICES AND GAN MONOLITHIC INTEGRATION

Timing & location
Monday, December 9, 1:30 p.m.
Continental Ballroom 1-3

Co-Chairs
P. Moens, ON Semiconductor
G. Prechtl, Infineon Technologies

Session 4.4 (3:15 p.m.)

GaN-on-SOI: Monolithically Integrated All-GaN ICs for Power Conversion (Technical paper)

We report the first comprehensive research about GaN power ICs on GaN-on-SOI. HEMT, MIM capacitor, SBD, 2DEG resistor, and resistor-transistor logic (RTL) are co-integrated. A 48V-to-1V buck converter is realized using 200 V GaN half-bridges with integrated drivers. Further, an all-GaN buck converter is successfully designed using the GaN PDK.

Main author
Xiangdong Li

Co-authors
Nooshin Amirifar, Karen Geens, Ming Zhao, Weiming Guo, Hu Liang, Shuzhen You, Niels Posthuma, Brice De Jaeger, Steve Stoffels, Benoit Bakeroot, Dirk Wellekens, Benjamin Vanhove, Thibault Cosnier, Robert Langer, Denis Marcon, Guido Groeseneken, Stefaan Decoutere, imec, KU Leuven

> Working at imec, I can focus on my research project - instead of having to worry about the financials. Imec combines academic excellence with innovative ideas and a unique research infrastructure; this allows science enthusiasts like myself to explore a host of opportunities.

_Umberto Celano

SESSION 5

RELIABILITY OF SYSTEMS AND DEVICES - BACK END AND ADVANCED CHARACTERIZATION

Timing & location
Monday, December 9, 1:30 p.m.
Continental Ballroom 4

Co-Chairs
K. Weide-Zaage, Leibniz Universität Hannover
G. Reimbold, CEA-LETI

Session 5.1 (1:35 p.m.)

Reverse Tip Sample Scanning for Precise and High-Throughput Electrical Characterization of Advanced Nodes (Technical paper)

A new method is proposed to enable high-throughput and high-resolution electrical atomic force microscopy in nanoelectronics. Using a reversed pathway of operation, our technique yields an increased time-to-data (>10x), enhanced dataset statistics and nm-precise resolution; as herein demonstrated for two and three-dimensional carrier profiling in fin structures of advanced nodes.

Main author
Umberto Celano

Co-authors
Thomas Hantschel, Thijs Boehme, Antti Kanniainen, Lennaert Wouters, Hugo Bender, Niels Bosman, Chris Drijbooms, Steven Folkersma, Kristof Paredis, Wilfried Vandervorst, Paul van der Heide, imec, KU Leuven, University of Jyväskylä

SESSION 9

MICROWAVE, MILLIMETER WAVE AND ANALOG TECHNOLOGY - COMPOUND SEMICONDUCTORS AND NOVEL MATERIALS FOR RF AND MMWAVE

Timing & location
Monday, December 9, 1:30 p.m.
Imperial Ballroom A

Co-Chairs
M. Urteaga, Teledyne Science
F. Gianesello, STMicroelectronics

Session 9.1 (1:35 p.m.)

First Demonstration of III-V HBTs on 300 mm Si Substrates Using Nano-Ridge Engineering (Technical paper)

In this paper, we demonstrate GaAs/InGaP HBTs grown on a 300 mm Si substrate. A DC current gain of ~112 and breakdown voltage, BVCBO of 10 V is achieved. The emitter-base and base-collector diodes show an ideality factor of ~1.2 and ~1.4, respectively. This demonstration shows the potential for enabling a hybrid III-V CMOS/ technology for 5G and mm-wave applications, not limited to GaAs but which can also be extended to InGaAs on a 300 mm Si substrate.

Main author
A.Vais

Co-authors
L. Witters, Y. Mols, A.S.-Hernandez, A. Walke, H. Yu, M. Baryshnikova, G. Mannaert, V. Deshpande, R. Alcotte, M. Ingels, P. Wambacq, B. Parvais, R. Langer, B. Kunert, N. Waldron, and N. Collaert, imec, KU Leuven, VUB

SESSION 10

SENSORS, MEMS AND BIOELECTRONICS/ OPTOELECTRONICS, DISPLAYS, AND IMAGERS FOCUS SESSION: HUMAN MACHINE INTERFACE

Timing & location
Monday, December 9, 1:30 p.m.
Imperial Ballroom B

Co-Chairs
H. Lee, KAIST
A. Tournier, STMicroelectronics

Session 10.1 (1:35 p.m.)

The Neuropixels Probe: A CMOS Based Integrated Microsystems Platform for Neuroscience and Brain-computer Interfaces (Invited)

CMOS enabled high-density electrophysiology probes are enabling transformational neuroscience experiments, e.g., single neuron precision, multi region, neuronal activity recording. They have enabled recording in multi-probe experiments with large neuronal populations (> 3000 neurons). Initial studies in primates indicate their transformational potential in brain computer interfaces and research in neural disorders.

Main author
Barundeb Dutta

Co-authors
Alexandru Andrei, Timothy Harris, Carolina Mora-Lopez, John O'Callaghan, Jan Putzeys, Bogdan Raducanu, Simone Severi, Sergey Stavisky, Eric Trautmann, Marleen Welkenhuysen, Krishna Shenoy, imec, Stanford University, HHMI Janelia Research Campus

TUESDAY, DECEMBER 10

SESSION 11

ADVANCED LOGIC TECHNOLOGY - GATE-ALL-AROUND DEVICE TECHNOLOGIES

Timing & location
Tuesday, December 10, 9:00 a.m.
Grand Ballroom A

Co-Chairs
S. Maitrejean, CEA
K.H. Cho, Samsung

Session 11.1 (9:05 a.m.)

Vertical Nanowire and Nanosheet FETs: Device Features, Novel Schemes for Improved Process Control and Enhanced Mobility, Potential for Faster & More Energy-Efficient Circuits (Technical paper)

We report on p&n vertical gate-all-around nanowire and nanosheet FETs, evaluating the impact of doping and key dimensions on: performance, variability, noise, reliability (junctionless vs. inversionmode) using RMG, which enables a new scheme for enhanced mobility by stress. Gate (mis) alignment control and their potential as MRAM selector are also discussed.

Main author
Anabela Veloso

Co-authors
Geert Eneman, Trong Huynh-Bao, Adrian Chasin, Eddy Simoen, Emma Vecchio, Katia Devriendt, Stephan Brus, Erik Rosseel, Andriy Hikavyy, Roger Loo, Vasile Paraschiv, BT Chan, Dunja Radisic, Waikin Li, J. J. Versluijs, Lieve Teugels, Farid Sebaai, Paola Favia, Hugo Bender, Eric Vancoille, Jeroen E. Scheerder, Claudia Fleischmann, Naoto Horiguchi, P. Matagne, imec

Session 11.3 (9:55 a.m.)

3D-carrier Profiling and Parasitic Resistance Analysis in Vertically Stacked Gate-All-Around Si Nanowire CMOS Transistors (Technical paper)

We have utilized s-SSRM in order to extract for the first time 3D carrier distributions into multi-channel h-GAA Si NW-CMOSFETs. Good correlation with DIBL characteristics could be established. Thanks to these results and to TCAD simulations we could give a first explanation of the ON-current performance increase of GAA pMOSFETs.

Main author
Pierre Eyben

Co-authors
Romain Ritzenthaler, An De Keersgieter, Umberto Celano, Thomas Chiarella, Anabela Veloso, Hans Mertens, Vanessa Pena, Gaetano Santoro, Jerome Machillot, Myungsun Kim, Toshihiko Miyashita, Naomi Yoshida, Hugo Bender, Olivier Richard, Kristof Paredis, Lennaert Wouters, Jerome Mitard, Naoto Horiguchi, imec, Applied Materials

SESSION 13

RELIABILITY OF SYSTEMS AND DEVICES - FOCUS SESSION: RELIABILITY AND SECURITY IN CIRCUITS AND SYSTEMS

Timing & location
Tuesday, December 10, 9:00 a.m.
Continental Ballroom 4

Co-Chairs
G. Konstadinidis, Google
G. Sethi, Amazon

Session 13.4 (10:20 a.m.)

Security and Reliability – Friend or Foe (Invited)

Security and reliability are more closely related than one might expect. This paper studies interesting research topics at the boundaries between the two domains. Reliability concerns can benefit security, e.g. to improve the performance of PUFs. Reliability issues can also trigger new security breaches, e.g. enabling Rowhammer attacks.

Main author
Ingrid Verbauwhede

Co-authors
Kai-Hsin Chuang, KU Leuven, imec

SESSION 15

MEMORY TECHNOLOGY - FERROELECTRICS

Timing & location
Tuesday, December 10, 9:00 a.m.
Continental Ballroom 6

Co-Chairs
J. Van Houdt, imec/KU Leuven
M. Kobayashi, University of Tokyo

Session 15.6 (11:35 a.m.)

Impact of Charge Trapping on Imprint and its Recovery in HfO2 based FeFET (Technical paper)

For ferroelectric-HfO2 based FET (FeFET), imprint has been regarded as a major issue. However, most studies have been conducted only on capacitors. In this paper, imprint of FeFET as well as simulation of charge trapping is reported. The strong effect of charge trapping is responsible for imprint and its recovery.

Main author
Yusuke Higashi

Co-authors
Nicolò Ronchi, Ben Kaczer, Kaustuv Banerjee, Sean McMitchell, Barry O'Sullivan, Sergiu Clima, Albert Minj, Umberto Celano, Luca DiPiazza, Masamichi Suzuki, Dimitri Linten, Jan Van Houdt, Kioxia Corporation, imec, KU Leuven

SESSION 16

OPTOELECTRONICS, DISPLAYS, AND IMAGERS - IMAGE SENSORS

Timing & location
Tuesday, December 10, 9:00 a.m.
Continental Ballroom 7-9

Co-Chairs
A. Tournier, STMicroelectronics
P. Malinowski, imec

Pawel Malinowski (Co-Chair)
Program Manager User Interfaces & Imagers, imec

SESSION 17

MICROWAVE, MILLIMETER WAVE AND ANALOG TECHNOLOGY - III-NITRIDE DEVICES AND CO-INTEGRATION

Timing & location
Tuesday, December 10, 9:00 a.m.
Imperial Ballroom A

Co-Chairs
D. Meyer, Naval Research Laboratory
N. Collaert, imec

Session 17.2 (9:30 a.m.)

CMOS-compatible GaN-based Devices on 200mm-Si for RF Applications: Integration and Performance (Technical paper)

We report on the integration, and optimization of Al(Ga,In)N HEMTs, MISHEMTs and MOSFETs on 200-mm Si wafers using Au-free, CMOS compatible processing, and discuss performance tradeoffs, limitations and solutions. We show that MISHEMTs have the potential to outperform the other device types in terms of device scalability for high-frequency operation.

Main author
Uthayasankaran Peralagu

Co-authors
AliReza Alian, Vamsi Putcha, Ahmad Khaled, Raul Rodriguez, Arturo Sibaya-Hernandez, Shane Chang, Eddy Simoen, Simeng Zhao, Brice De Jaeger, Daniel Fleetwood, Piet Wambacq, Ming Zhao, Bertrand Parvais, Niamh Waldron, Nadine Collaert, imec, KU Leuven, National Chiao Tung, Vanderbilt University, Vrije Universteit Brussels

SESSION 18

SENSORS, MEMS AND BIOELECTRONICS - BIOMEDICAL SENSORS AND NEURAL INTERFACES

Timing & location
Tuesday, December 10, 9:00 a.m.
Imperial Ballroom B

Co-Chairs
G. Xu, University of Massachusetts, Amherst
S. Zafar, IBM T.J. Watson Research Center

Session 18.4 (10:20 a.m.)

Design and Fabrication of CMOS-based Neural Probes for Large-scale Electrophysiology (Invited)

This paper describes the design and fabrication of the CMOS-based Neuropixels neural probe, which integrates a high-density micro-electrode array and a high channel count to enable large-scale electrophysiology in small rodents. Miniaturization and scalability aspects are also discussed here.

Main author
Carolina Mora Lopez

Co-authors
Alexandru Andrei, Shiwei Wang, Rita Van Hoof, Simone Severi, Nick Van Helleputte, imec

Session 18.6 (11:35 a.m.)

BioFET Technology: Aggressively Scaled pMOS FinFET as Biosensor (Technical paper)

We report for the first time on a BioFET sensor using 10nm wide FinFETs built in a 300 mm pilot line.
Median voltage referred 1/f noise is only ~500 µV2µm2Hz (@1Hz). pH sensitivity for HfO_2 is near the Nernstian limit. Biomolecular transduction is demonstrated for DNA grafting and PNA-DNA hybridization.

Main author
Koen Martens

Co-authors
Sybren Santermans, Mihir Gupta, Geert Hellings, Robin Wuytens, Bert Du Bois, Emmanuel Dupuy, Efrain Altamirano-Sanchez, Karolien Jans, Rita Vos, Tim Stakenborg, Liesbet Lagae, Marc Heyns, Simone Severi, Wim Van Roy, imec, KU Leuven

SESSION 19

ADVANCED LOGIC TECHNOLOGY - BEOL AND 3D PACKAGING INNOVATION

Timing & location
Tuesday, December 10, 2:15 p.m.
Grand Ballroom A

Co-Chairs
H. Shang, TSMC
C. Liu, National Taiwan University

Session 19.1 (2:20 p.m.)

Buried Power Rails and Back-side Power Grids: Arm® CPU Power Delivery Network Design Beyond 5nm (Technical paper)

An Arm CPU is designed with buried-power rails (BPR) and back-side power delivery at 3nm node. It is found that careful power-delivery-network design alleviates IR drop but deteriorates the energy with front side power delivery. However, back-side power delivery with BPR eliminates this trade-off demonstrating ~7X improvement in IR drop.

Main author
Divya Prasad

Co-authors
S. S. Teja Nibhanapudi, Shidhartha Das, Odysseas Zografos, Bilal Chehab, Satadru Sarkar, Rogier Baert, Alex Robinson, Anshul Gupta, Alessio Spessot, Peter Debacker, Diederik Verkest, Jaydeep Kulkarni, Brian Cline, Saurabh Sinha, Arm Reserarch, The University of Texas at Austin, imec

Session 19.3 (3:10 p.m.)

Three-Layer BEOL Process Integration with Supervia and Self-Aligned-Block Options for the 3nm Node (Technical paper)

The integration of a three-layer BEOL process with an intermediate 21nm pitch level, relevant for the 3nm node, is demonstrated using full barrier-less Ruthenium dual-damascene metallization. Variations of minimum island, via extension and tip-to-tip were electrically evaluated. Scaling boosters supervia and selfaligned block were investigated. Reliability study included.

Main author
Victor-Hugo Vega-Gonzalez

Co-authors
Christopher Wilson, Basoene Briggs, Stefan Decoster, J. J. Versluijs, Alicja Lesniewska, Sara Paolillo, Rogier Baert, Harinarayanan Puliyalil, Joost Bekaert, Els Kesters, Quoc Toan Le, Christophe Lorant, Olalla Varela Pedreira, Lieve Teugels, Nancy Heylen, Zaid El-Mekki, Marleen van der Veen, Tomas Webers, Hemant Vats, Luc Rijnders, Miroslav Cupak, Jae Uk Lee, Youssef Drissi, L. Halipre, A.-L. Charley, P. Verdonck, T. Witters, S. V. Gompel, Y. Kimura, N. Jourdan, I. Ciofi, A. Gupta, A. Contino, G. Boccardi, S. Lariviere, L. Dupas, B. De-Wachter, E. Vancoille, F. Lazzarino, M Ercken, P. Debacker, R. Kim, D. Trivkovic, K. Croes, P. Leray, L. Dillemans, Y.-F. Chen, Z. Tokei, imec

SESSION 20

POWER DEVICES AND SYSTEMS - SiC POWER DEVICES

Timing & location
Tuesday, December 10, 2:15 p.m.
Continental Ballroom 1-3

Co-Chairs
I. Kizilyalli, ARPA-E
D. Hisamoto, Hitachi

Session 20.5 (4:25 p.m.)

Physical Modeling of Bias Temperature Instabilities in SiC MOSFETs (Technical paper)

The performance of i MOSFETs can still not be fully exploited due to defects in the atomic structure giving rise to BTI. We investigate BTI in lateral and vertical channel nMOSFETs. By doing physics-based device simulations we extract defect bands which finally enables us to provide accurate lifetime extrapolations.

Main author
Christian Schleich

Co-authors
Judith Berens, Gerhard Rzepa, Gregor Pobegen, Gerald Rescher, Stanislav Tyaginov,Tibor Grasser, Michael Waltl, TU Vienna, kai, Global TCAD Solution GmbH, Infineon Technologies Austria AG, imec

SESSION 21

RELIABILITY OF SYSTEMS AND DEVICES - EMERGING TRANSISTOR RELIABILITY AND PERTINENT STRATEGIES

Timing & location
Tuesday, December 10, 2:15 p.m.
Continental Ballroom 4

Co-Chairs
F. Schanovsky, Global TCAD Solutions BmbH
B. Weir, Broadcom

Session 21.2 (2:45 p.m.)

A Physics-aware Compact Modeling Framework for Transistor Aging in the Entire Bias Space (Technical paper)

A unified compact modeling framework of device aging is proposed and verified on FinFET technology.

Main author
Zhicheng Wu

Co-authors
Jacopo Franco, Philippe Roussel, Stanislav Tyaginov, Brecht Truijen, Michiel Vandemaele, Geert Hellings, Nadine Collaert, Guido Groeseneken, Dimitri Linten, Ben Kaczer, imec, KU Leuven

SESSION 21

RELIABILITY OF SYSTEMS AND DEVICES - EMERGING TRANSISTOR RELIABILITY AND PERTINENT STRATEGIES

Timing & location
Tuesday, December 10, 2:15 p.m.
Continental Ballroom 4

Co-Chairs
F. Schanovsky, Global TCAD Solutions BmbH
B. Weir, Broadcom

Session 21.3 (3:10 p.m.)

Understanding and Physical Modeling Superior Hot-Carrier Reliability of Ge pNWFETs (Technical paper)

We accurately model degradation and the time-to-failure measured during hot-carrier stress in Ge and Si pNWFETs. The superior time-to-failure in Ge devices has been explained by a much higher energy (5.5eV) needed to break Ge-O bonds (precursors) and form O-vacancies (defects) compared to the Si-H bond rupture energy (2.6eV).

Main author
Stanislav Tyaginov

Co-authors
Al-Moatasem El-Sayed, Alexander Makarov, Adrian Chasin, Hiroaki Arimura, Michiel Vandemaele, Markus Jech, Elena Capogreco, Liesbeth Witters, Alexander Grill, An De Keersgieter, Geert Eneman, Dimitri Linten, Ben Kaczer, imec, Nanolayers, TU Vienna

Session 21.6 (4:50 p.m.)

Physical Insights on Steep Slope FEFETs including Nucleation-Propagation and Charge Trapping (Technical paper)

We present an analysis of steep slope FEFETs including statistical multi-domain nucleation-propagation and high-K hafnia-oxide charge trapping, based on a compact model validated on transistor I-V measurement. The proposed field-independent propagation proves key to explaining the steep slope. Trapping is shown to assist polarization-switching and enlarge the detrimental I-V hysteresis.

Main author
Yang Xiang

Co-authors
Marie Garcia Bardon, Md Nur Kutubul Alam, Mischa Thesberg, Ben Kaczer, Philippe Roussel, Mihaela Ioana Popovici, Lars-Ake Ragnarsson, Brecht Truijen, Anne S. Verhulst, Bertrand Parvais, Naoto Horiguchi, Guido Groeseneken, J. Van Houdt, imec, KU Leuven, Vrije Universteit Brussel, TU Wien

SESSION 22

MEMORY TECHNOLOGY/EMERGING DEVICE AND COMPUTE TECHNOLOGY - FOCUS SESSION: EMERGING AI HARDWARE

Timing & location
Tuesday, December 10, 2:15 p.m.
Continental Ballroom 5

Co-Chairs
C. Petti, Sunrise Memory, Inc.
T-H Hou, National Chiao Tung University

Session 22.2 (2:45 p.m.)

Towards 10000TOPS/W DNN Inference with Analog in-Memory Computing – A Circuit Blueprint, Device Options and Requirements (Invited)

This paper presents a circuit blueprint for a 10000TOPS/W matrix-vector multiplier for neural network inference based on Analog in-Memory Computing, using pulse-width encoded activations and precharge discharge summation lines. Three suited device options are discussed: SOT-MRAM, IGZO-based 2T1C DRAM gain cell, and projection PCM with separate write path.

Main author
Stefan Cosemans

Co-authors
Bram Verhoef, Jonas Doevenspeck, Ioannis Papistas, Francky Catthoor, Peter Debacker, Arindam Mallik, Diederik Verkest, imec, KU Leuven

SESSION 23

EMERGING DEVICE AND COMPUTE TECHNOLOGY - EMERGING DEVICES FOR EXTENDING MOORE'S LAW

Timing & location
Tuesday, December 10, 2:15 p.m.
Continental Ballroom 6

Co-Chairs
Y. Chai, The Hong Kong Polytechnic University
T. Mueller, Vienna University of Technology

Session 23.2 (2:45 p.m.)

Ultra-scaled MOCVD MoS_2 MOSFETs with 42nm Contact Pitch and 250µA/µm Drain Current (Technical paper)

For CVD MoS_2 FETs we demonstrate that downscaling the top-contact length to 13nm induces no penalty on the characteristics, experimentally confirming edge injection with I_{on}=250µA/µm for 50nm SiO_2 gate oxide. This is equally valid for thinner 4nm HfO_2 gate oxide, where the switching characteristics improve with SS_{min}=80mV/dec

Main author
Quentin Smets

Co-authors
Goutham Arutchelvan, Julien Jussot, Devin Verreck, Inge Asselberghs, Ankit Nalin Mehta, Abhinav Gaur, Dennis Lin, Salim El Kazzi, Benjamin Groven, Matty Caymax, Iuliana Radu, imec, KU Leuven

> I enjoy working at imec because here I can do in-depth research, using cutting-edge infrastructure and being utmost relevant to the semiconductor industry. Also, as imec is growing quickly and continuously calling upon its employees to drive change forward, a true sense of engagement and belonging is created.

_Quentin Smets

SESSION 24

MODELING AND SIMULATION - AB INITIO SIMULATION OF MATERIALS, DEVICES, AND INTERCONNECTS

Timing & location
Tuesday, December 10, 2:15 p.m.
Continental Ballroom 7-9

Co-Chairs
B. Magyari-Kope, TSMC
V. Georgiev, University of Glasgow

Session 24.1 (2:20 p.m.)

First-Principles Parameter-Free Modeling of n- and p-FET Hot-Carrier Degradation (Technical paper)

We present and validate a quantum chemistry approach to capture the intricate nature of hot-carrier degradation, which is essentially free of fit parameters. The newly identified resonance scattering mechanism allows us to clearly reveal the differences between degradation in n- and p-channel devices.

Main author
Markus Jech

Co-authors
Stanislav Tyaginov, Ben Kaczer, Jacopo Franco, Dominic Jabs, Christoph Jungemann, Michael Waltl, Tibor Grasser, TU Wien, imec, RWTH Aachen University

WEDNESDAY, DECEMBER 11

SESSION 29

ADVANCED LOGIC TECHNOLOGY - HIGH MOBILITY GE-BASED CHANNEL DEVICES

Timing & location
Wednesday, December 11, 9:00 a.m.
Grand Ballroom B

Co-Chairs
Y. Zhao, Zhejiang University
T. Yamaguchi, Renesas Electronic Corp.

Session 29.2 (9:30 a.m.)

Ge Oxide Scavenging and Gate Stack Nitridation for Strained Si0.7Ge0.3 pFinFETs Enabling 35% Higher Mobility than Si (Technical paper)

We have demonstrated multiple ways to reduce the D_{IT} of Si-cap-free low-Ge-content (25-30%) SiGe gate stack. The D_{IT} is reduced by Ge oxide scavenging, nitridation and optimized high-pressure anneal. 8-nmwide strained scaled $Si_{0.7}Ge_{0.3}$ pFinFET with the optimized gate stack demonstrated 35% mobility improvement over Si counterpart.

Main author
Hiroaki Arimura

Co-authors
Kurt Wostyn, Lars-Ake Ragnarsson, Elena Capogreco, Adrian Chasin, Thierry Conard, Stephan Brus, Paola Favia, Jacopo Franco, Jerome Mitard, Steven Demuynck, Naoto Horiguchi, imec

Session 29.4 (10:20 a.m.)

Enabling Sub-5nm CMOS Technology Scaling: Thinner and Taller! (Invited)

Scaling beyond 5nm will bring us into the post FinFET era where new device architectures optimized for CMOS logic scaling will be required. In this paper, the evolution to vertically stacked Nanosheets, Forksheet, and finally CFET are reviewed in conjunction with buried power rails and wrap around contact.

Main author
Julien Ryckaert

Co-authors
Myung Hee Na, Pieter Weckx, Doyoung Jang, Pieter Schuddinck, Bilal Chehab, Sudhir Patli, Satadru Sarkar, Odysseas Zografos, Rogier Baert, Diederik Verkest, imec

SESSION 31

EMERGING DEVICE AND COMPUTE TECHNOLOGY - FOCUS SESSION: QUANTUM COMPUTING INFRASTRUCTURE

Timing & location
Wednesday, December 11, 9:00 a.m.
Continental Ballroom 5

Co-Chairs
I. Radu, imec
Z. Chen, Purdue University

Iuliana Radu (Co-Chair)
Director of Quantum and Exploratory Computing, imec

SESSION 32

MODELING AND SIMULATION - MODELING OF EMERGING MEMORY SYSTEMS

Timing & location
Wednesday, December 11, 9:00 a.m.
Continental Ballroom 6

Co-Chairs
N. Xu, Samsung
B. Gao, Tsinghua University

Session 32.1 (9:05 a.m.)

Quantitative 3-D Model to Explain Large Single Trap Charge Variability in Vertical NAND Memory (Technical paper)

We present a TCAD model that reproduces large single trap V_T-shifts (>100mV) in 3-D NAND through targeted charge placement based on linear response. With this model, we investigate worst-case V_T-shifts in terms of bias conditions and junction position and we outline a sampling strategy that allows to reproduce experimental distributions.

Main author
Devin Verreck

Co-authors
Antonio Arreghini, Joao Bastos, Franz Schanovsky, Ferdinand Mitterbauer, Christian Kernstock, Markus Karner, Robin Degraeve, Geert Van den bosch, Arnaud Furnemont, imec, Global TCAD Solutions GmbH

SESSION 33

OPTOELECTRONICS, DISPLAYS, AND IMAGERS - SILICON PHOTONICS

Timing & location
Wednesday, December 11, 9:00 a.m.
Continental Ballroom 7-9

Co-Chairs
A. Giesecke, AMO
S. Matsuo, NTT

Session 33.5 (10:45 a.m.)

2D-3D Integration of High-K Dielectric with 2D Heterostructures for Optoelectronic Applications (Invited)

Graphene-based devices are edging closer to industrialization, at first instance related to sensors and opto-electronics applications. In particular, graphene-based photodetectors and modulators have already shown competitive performances and proof-on-concept integration with Si-CMOS technologies has been demonstrated. For example, graphene modulators are reaching, and even surpassing, state-of-the-art commercial modulators. In order to fulfil all industrial requirements, new dielectric combinations providing flat encapsulation for graphene that allow high levels of doping control and hysteresis-free operation are needed.

Main author
B. Terrés

Co-authors
H. Agarwal, L. Orsini, A. Montanaro, V. Sorianello, D. van Thourhout, K. Watanabe, T. Taniguchi, M. Romagnoli and F. H. L. Koppens, The Barcelona Institute of Science and Technology, Photonic Networks and Technologies National Laboratory, University–IMEC, National Institute for Material Science, ICREA

> Working at imec offers great opportunities for professional and personal growth. Thanks to imec's state-of-the-art infrastructure, and in close contact with our industry and academic partners, we develop the next generation of semiconductor technologies.

_Daniele Garbin

SESSION 35

MEMORY TECHNOLOGY - SELECTORS AND RRAM: TECHNOLOGY AND COMPUTING

Timing & location
Wednesday, December 11, 1:30 p.m.
Grand Ballroom A

Co-Chairs
H-Y Cheng, Macronix International Co., Ltd.
S. Spiga, CNR-IMM

Session 35.1 (1:35 p.m.)

Composition Optimization and Device Understanding of Si-Ge-As-Te Ovonic Threshold Switch Selector with Excellent Endurance (Technical paper)

We explore the composition space of the Si-Ge-As-Te based ovonic threshold switch selector device. We optimize the composition to increase the crystallization temperature T_x >450°C and achieve stable endurance of more than 10_{11} cycles. We propose a switching model that predicts the distribution of the threshold voltage, drift and time-dependent instabilities.

Main author
Daniele Garbin

Co-authors
Wouter Devulder, Robin Degraeve, Gabriele Luca Donadio, Sergiu Clima, Karl Opsomer, Andrea Fantini, Daniel Cellier, Wan Gee Kim, Mahendra Pakala, Andrew Cockburn, Christophe Detavernier, Romain Delhougne, Ludovic Goux, Gouri Sankar Kar, imec, Applied Materials, Inc., Ghent University

SESSION 35

MEMORY TECHNOLOGY - SELECTORS AND RRAM: TECHNOLOGY AND COMPUTING

Timing & location
Wednesday, December 11, 1:30 p.m.
Grand Ballroom A

Co-Chairs
H-Y Cheng, Macronix International Co., Ltd.
S. Spiga, CNR-IMM

Session 35.2 (2:00 p.m.)

Endurance Improvement of More than Five Orders in $GexSe1-_x$ OTS Selectors by using a Novel Refreshing Program Scheme (Technical paper)

OTS degradation and the endurance can be therefore improved by more than five orders without adding additional material elements or process steps, based on understanding of the recoverable (slow delocalized defects) and non-recoverable (Ge-Se segregation/crystallization) degradation mechanisms.

Main author
Firas Hatem

Co-authors
Zheng Chai, Weidong Zhang, Andrea Fantini, Robin Degraeve, Sergiu Clima, Daniele Garbin, John Robertson, Yuzheng Guo, Jian Fu Zhang, John Marsland, Pedro Freitas, Ludovic Goux, Gouri Sankar Kar, imec, Liverpool John Moores University, University of Cambridge, Wuhan University

> As a researcher in the domain of memory devices, I have always aimed at combining my scientific expertise with an application-oriented approach, and imec is a unique research center in this regard. Thanks to its results-driven mentality, its highly international environment and its top-level infrastructure, imec is an ideal place for developing my career, providing me with access to cutting-edge processes and technologies. Besides, imec's world-renowned reputation enables a direct interaction with world-leading experts in all semiconductor fields, strongly enriching my scientific background.

_Attilio Belmonte

SESSION 35

MEMORY TECHNOLOGY - SELECTORS AND RRAM: TECHNOLOGY AND COMPUTING

Timing & location
Wednesday, December 11, 1:30 p.m.
Grand Ballroom A

Co-Chairs
H-Y Cheng, Macronix International Co., Ltd.
S. Spiga, CNR-IMM

Session 35.8 (4:30 p.m.)

Co Active Electrode Enhances CBRAM Performance and Scaling Potential (Technical paper)

We report for the first time the low-current performance enhancement combined with the improvement of the scaling potential in CBRAM devices by adopting Co as active electrode. Co is proven to yield, with respect to Cu, faster/lower voltage switching and more stable conductive filaments.

Main author
Attilio Belmonte

Co-authors
Janaki Radhakrishnan, Ludovic Goux, Gabriele Luca Donadio, P. Kumbhare, Augusto Redolfi, Romain Delhougne, Laura Nyns, Wouter Devulder, Thomas Witters, Angelo Covello, Alexis Franquet, Valentina Spampinato, Shreya Kundu, Ming Mao, Hubert Hody, Gouri Sankar Kar, Guy Vereecke, imec, KU Leuven, Università della Calabria

SESSION 36

ADVANCED LOGIC TECHNOLOGY - CMOS PLATFORM TECHNOLOGIES

Timing & location
Wednesday, December 11, 1:30 p.m.
Grand Ballroom B

Co-Chairs
C. Chu, Applied Materials
Y. Li, Lam Research

Session 36.2 (2:00 p.m.)

Variability Sources in Nanoscale Bulk FinFETs and TiTaN- a Promising Low Variability WFM for 7/5nm CMOS Nodes (Technical paper)

An experimental methodology to segregate variability sources in FinFETs (W_{fin} <10nm) is proposed. The V_t variation, from gate work-function metal (WFM) and oxide charge variations, is the major contributor to in-wafer variability. The FER, GER, RDF contribution to V_t variability is negligible. TiTaN, low variability WFM, for future gate-stack, is introduced.

Main author
Mandar S. Bhoir

Co-authors
Thomas Chiarella, Lars-Ake Ragnarsson, Jerome Mitard, Naoto Horiguchi, Nihar Ranjan Mohapatra, IIT Gandhinagar, imec

> “Before joining academia in the mid 80s, I spent a couple of years at imec. This truly helped me understand what it means to reach for the stars while at the same time having both of your feet firmly grounded in reality. While imec was already an exciting place to be 30 years ago, it is exponentially even more so today. There are not many places in the world that cover the range of manufacturing, device, circuit and system technologies that imec is covering. Hence if I were you and I would have this dream, I would not hesitate and apply for an imec ‘tenure track’ position!

_Jan Rabaey CTO System-Technology Co-Optimization, imec (Berkeley office)

> I joined imec as a PhD student working on transistor reliability. Currently, I am in charge of design and technology co-optimizations for future logic and SRAM memories. Imec's interdisciplinary and open working environment allows individuals to pursue a unique career – across a multitude of research domains.

_Pieter Weckx

SESSION 36

ADVANCED LOGIC TECHNOLOGY - CMOS PLATFORM TECHNOLOGIES

Timing & location
Wednesday, December 11, 1:30 p.m.
Grand Ballroom B

Co-Chairs
C. Chu, Applied Materials
Y. Li, Lam Research

Session 36.5 (3:15 p.m.)

Novel Forksheet Device Architecture as Ultimate Logic Scaling Device Towards 2nm (Technical paper)

Due to CPP scaling slowdown below 42nm, several scaling boosters are needed to reduce the logic standard cell height. Limited scaling can be achieved using FinFET and nanosheets due integration limits for PN separation. A novel forksheet device is proposed achieving extremely scaled PN space using limited additional processing complexity.

Main author
Pieter Weckx

Co-authors
Julien Ryckaert, Eugenio Litta, Dmitry Yakimets, Philippe Matagne, Pieter Schuddinck, Doyoung Jang, Bilal Chehab, Rogier Baert, Mohit Gupta, Yusuke Oniki, Lars-Ake Ragnarsson, Naoto Horiguchi, Alessio Spessot, Diederik Verkest, imec

> Working at imec has been a fabulous experience! Its unique research infrastructure, broad expertise and the collaborative environment have strongly helped me to find innovative solutions in the domain of quantum computing. The diversity of imec's staff makes for a very productive working environment.
>
> **_Fahd Ayyalil Mohiyaddin**

SESSION 39

MODELING AND SIMULATION - MULTISCALE MODELING OF DEVICES AND CIRCUITS

Timing & location
Wednesday, December 11, 1:30 p.m.
Continental Ballroom 6

Co-Chairs
W. Vandenberghe, University of Texas, Dallas
C. Weber, Intel

Session 39.5 (3:15 p.m.)

Multiphysics Simulation & Design of Silicon Quantum Dot Qubit Devices (Technical paper)

Silicon qubits are strong contenders for building a large-scale quantum processor. Here, we combine several multiphysics simulation methods to assemble a design methodology for silicon qubit devices. We summarize key device parameters, dimensions and voltages based on detailed models that consider device electrostatics, stress, micro-magnetic

Main author
Fahd Ayyalil Mohiyaddin

Co-authors
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ABOUT imec

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