3.6 A 40nm CMOS Highly Linear 0.4-to-6GHz Receiver Resilient to 0dBm Out-of-Band Blockers

Jonathan Borremans[1], Gunjan Mandal[1], Vito Giannini[1], Tomohiro Sano[2], Mark Ingels[1], Bob Verbruggen[1], Jan Craninckx[1]

[1]imec, Leuven, Belgium, [2]Renesas Electronics, Itami, Japan

SDRs come of age ([1,2]) and transcend beyond just acquiring the reconfigurability to replace any standard radio: they develop toward systems where a simplified antenna interface can be used, with most dedicated filtering removed. This requires a receiver accommodating much higher linearity and resilience against out-of-band interference than a standard radio, still achieving competitive sensitivity (especially in the absence of interference). Mixer-first front-ends with excellent linearity have been reported [3]. However, their NF (including 1/f in absence of the LNA gain) is not competitive, and they may suffer from large LO feedthrough to the antenna (LOFT). Moreover they lack receiver functionality such as gain and filtering, which cannot be simply added without compromising linearity. A receiver with mixer-at-the-antenna-based bandpass filter [4] similarly may suffer from LOFT and increased NF. This work presents a full software-defined receiver with 3dB NF that tolerates 0dBm blockers with acceptable blocker NF at maximum gain. It achieves +10dBm out-of-band (OB) IIP3 and >+70dBm IIP2. Such a receiver is to operate using no other than harmonic-rejection filtering.

The blocker-resilient receiver architecture is depicted in Fig. 3.6.1. The main-path RF front-end embodies a linear LNA and *voltage-sampling* mixer. An RF blocker filter *at the LNA output* is formed by low-pass reconfigurable differential sampling capacitor C_{BB} which turns into a bandpass filter at RF centered around the LO frequency. Indeed, a passive mixer upconverts the impedance at the baseband terminals to the RF side [4-6]. Hence, a baseband cut-off at 2MHz provides low impedance for out-of-band blockers at RF beyond 2MHz from the carrier. In this work, the cut-off tunes from 1.5 to over 20MHz, and filters a blocker at 20MHz offset by about 15dB. The voltage sampling offers a *high* impedance in-band, unlike the low-impedance case in [1,2,4], which has a benign effect on NF, while out-of-band linearity benefits from the RF bandpass filtering.

Since in this architecture blocker filtering occurs at the LNA output, the latter should carry the input blocker to the output without compressing. To handle blockers up to 0dBm *at the input and internal nodes of the LNA* with such high linearity, the headroom of a 2.5V supply is leveraged. Dedicated startup circuitry in Fig. 3.6.2 ensures that no terminal-to-terminal voltages over the triple-well devices exceed the technology reliability limits: neither during start-up, nor during standard operation. Consequently, reliability is not jeopardized. At startup the LNA bias is enabled first, next the startup circuitry provides the supply causing the internal LNA nodes to ramp up to their operating point. The startup circuitry never enables the internal supply when the LNA is not biased properly (e.g. in absence of the 1.1V supply).

A capacitive cross-coupled common-gate LNA provides moderately low noise (2.5dB) for high linearity (~+10dBm IIP3) since no passive voltage amplification occurs at the input [7]. A small low-Q inductor provides shunt peaking for relatively wideband operation. The LNA is centered at 0.7 to 3GHz: out of this band NF is less imperative. The front-end provides ample gain (~15dB) to suppress the noise of the receiver's baseband, and 2b gain selection through switched R_{LG}.

When lower RF gain is needed at low NF, a mixer-first mode [3] can be activated by enabling LO_2 in Fig. 3.6.1. In this mode LO_1 is disabled, and so is the standard mixer by opening its switches. The bypass mixer reuses the relatively big filtering capacitor C_{BB}. Input matching is now provided by the parallel impedance of both mixer and LNA. The latter is reconfigured to draw less current (less g_m) and to provide the now higher required input impedance (see Fig. 3.6.2). At this lower RF gain the G_m of the first baseband stage is increased to suppress baseband noise (especially 1/f).

In mixer-first mode, the translational effect of the mixer and capacitor (Fig. 3.6.1) filters out-of-band blockers directly at the antenna. Nevertheless, since the mixer targets operation up to 6GHz, the tolerable switch size is limited. The switch resistance, which limits the lower bound of the out-of-band impedance provided by the mixer-based filter, therefore hardly provides an impedance lower than 50Ω. Consequently the filtering profile at the antenna is limited to just a few dB. A NF down to 6.5dB is attained (better than when lowering the LNA gain further), with proper linearity. The advantage of the configuration in this work, is that the mixer-first operation can be disabled when not required, while the additional area of the system is a mere eight switches and a set of LO drivers. Elegantly, the LNA bypass switch *is* the auxiliary mixer, which avoids linearity issues associated to other LNA bypass solutions.

IIP2 of both mixers, important for modulated blockers and cross-modulation in an SDR, can be calibrated through a voltage DAC adjusting the gate bias voltage of the switches (Fig. 3.6.4). Calibration (which can be done by TX loop-back) with I- and Q-DAC boosts IIP2 independently on both channels to levels in excess of +70dBm.

The voltage sampling front-end sets severe challenges on OB linearity (+20dBm) and noise (1nV/√Hz) of the first baseband stage, not to degrade the achieved front-end's performance in the full receiver chain. A variable G_m stage followed by a 2nd-order filtering TIA biquad addresses these requirements. It provides a linear high-input-impedance interface as well as initial conditioning of the signal for the rest of the chain. A passive pole, G_m-C filter and VGA finalize the receive chain. Together with the mixer pole formed by C_{BB}, 6th-order filtering is provided. The baseband tunes from 0.4 to 30MHz and <0-to-55dB gain. Similar to [1], a 6-to-12GHz fractional-N PLL with divider chain offers any possible 100MHz-to-6GHz quadrature LO. A 25% duty-cycle generator delivers either LO_1 or LO_2.

The receiver has been implemented in 40nm LP digital CMOS (Fig. 3.6.7). It consumes 30 to 55mW and 30 to 40mA in the PLL. Figure 3.6.3 reports conversion gain (70/60dB), S_{11} and NF (3/6.5dB) in LNA-/mixer-first mode. The excellent IB/OB-IIP3 are +6/+10dBm respectively, and the calibrated IIP2 exceeds +70dBm. The EVM is 3%. The 1dB blocker compression point $B_{1dB,CP}$ [2] vs. baseband frequency in Fig. 3.6.5 reaches -8dBm at 20MHz offset (similar for mixer-1st) at highest gain, limited by baseband. It improves to -5.5dBm with 6dB baseband gain back-off with no impact on NF. Naturally $B_{1dB,CP}$ tracks the RF and baseband filtering profile. LO leakage to antenna in mixer-1st operation is lower than -65dBm, below the 3GGP specification.

Finally, Fig. 3.6.5 shows blocker NF, limited by – amongst others – reciprocal mixing of blocker and LO phase noise. With a 0dBm blocker at 20MHz offset, the blocker NF is below 15dB (e.g. 3GPP requirement). In [4], the NF is 15dB at 20MHz for a -5dBm blocker. This work therefore reports the receiver with highest blocker resilience for low NF, highest linearity and frequency range among the works in Fig. 3.6.6. Unlike other solutions, the receiver handles blockers well in any mode. It therefore needs not to be configured to a dedicated (noisy) blocker-tolerant mode.

Acknowledgements:
The authors acknowledge H. Suys, M. Libois and B. Debaillie.

References:

[1] M. Ingels, V. Giannini, J. Borremans, G. Mandal, B. Debaillie, P. Van Wesemael, T. Sano, T. Yamamoto, D. Hauspie, J. Van Driessche, J. Craninckx, "A 5mm² 40nm LP CMOS 0.1-to-3GHz multistandard transceiver", *ISSCC Dig. Tech. Papers*, pp. 458-459, Feb. 2010.

[2] Z. Ru, N. A. Moseley, E. Klumperink, B. Nauta, "Digitally Enhanced Software-Defined Radio Receiver Robust to Out-of-Band Interference", *J. Solid-State Circuits*, Vol. 44, No. 12, pp. 3359-3375, Dec. 2009.

[3] M. Soer, E. Klumperink, Z. Ru, F. E. van Vliet, B. Nauta, "A 0.2-to-2.0GHz 65nm CMOS receiver without LNA achieving >11dBm IIP3 and <6.5 dB NF", *ISSCC Dig. Tech. Papers*, pp.222-223, Feb. 2009.

[4] A. Mirzaie, A. Yazdi, Z. Zhou, E. Chang, P. Suri, H. Darabi, "A 65nm CMOS Quad-Band SAW-Less Receiver for GSM/GPRS/EDGE", *VLSI Dig. of Tech. Papers*, pp.179-180, June 2010.

[5] B. W. Cook, A. Berny, A. Molnar, S. Lanzisera, K. S. J. Pister, "Low-Power 2.4-GHz Transceiver With Passive RX Font-End and 400-mV Supply", *J. Solid-State Circuits*, Vol. 41, No. 12, pp. 2757-2766, Dec. 2006.

[6] J. Borremans, G. Mandal, B. Debaillie, V. Giannini, J. Craninckx, "A sub-3dB NF Voltage-Sampling Front-End with +18dBm IIP_3 and +2dBm Blocker Compression Point", *Proc. of ESSCIRC*, Sept. 2010.

[7] H. Darabi, "A Blocker Filtering Technique for SAW-Less Wireless Receivers", *IEEE J. Solid-State Circuits*, Vol. 42, No. 12, Dec. 2007.

 978-1-61284-302-5/11/$26.00

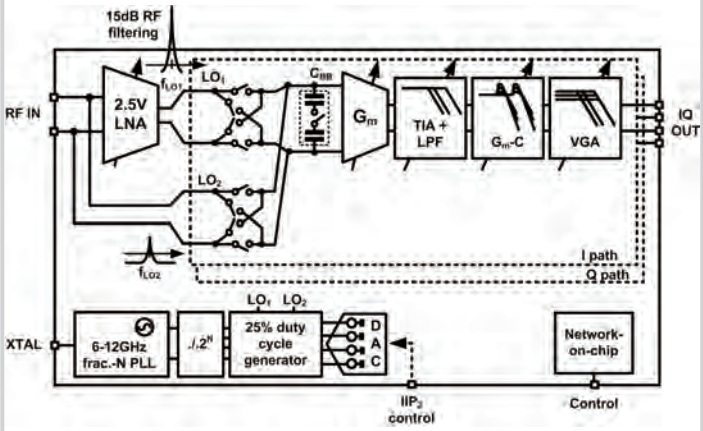

Figure 3.6.1: Highly linear software-defined receiver.

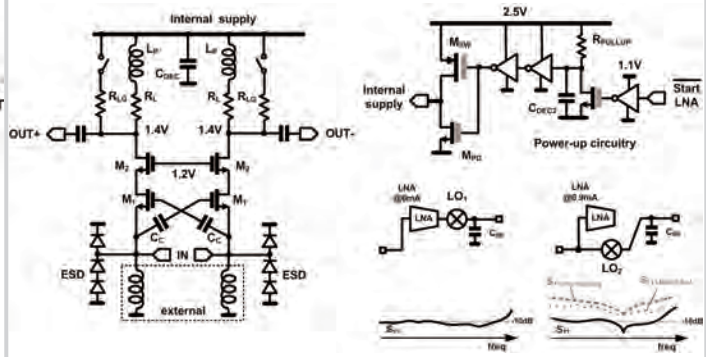

Figure 3.6.2: a) LNA schematic, (b) LNA start-up circuitry, (c) Input matching in LNA-first and mixer-first operation.

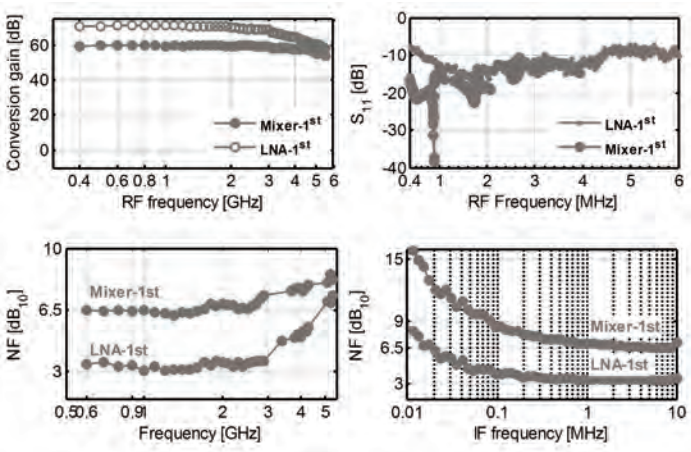

Figure 3.6.3: Measured conversion gain, S_{11}, NF of the receiver.

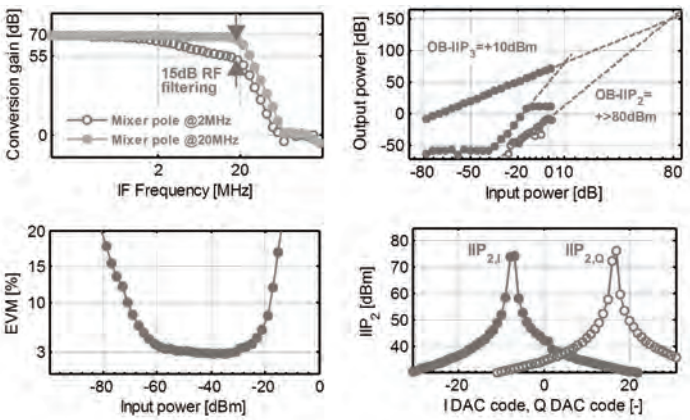

Figure 3.6.4: Measured conversion gain for baseband bandwidth set to 20MHz, EVM (64 subcarrier OFDM, 16QAM @2GHz), OB-IIP2/IIP3, and example IIP2 vs. calibration.

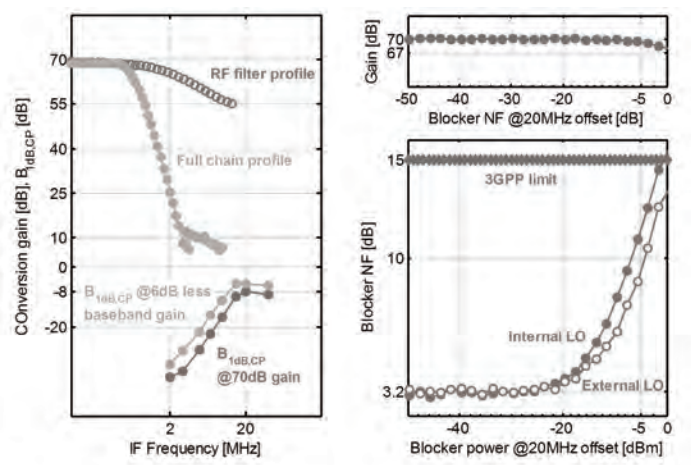

Figure 3.6.5: Blocker compression point at 70dB gain, filtering profile and measured compression and blocker NF vs. blocker power.

	This	Ingels [ISSCC'10]	Mirzaie [VLSI'10]	Bagheri [ISSCC'06]	Ru [JSSC'10]
Technology	**40nm**	40nm	65nm	65nm	65nm
System	**Full RX**	Full RX	Full RX	Full RX	Front-end
Frequency [GHz]	**0.4-6**	0.1-6	0.8-1.99	0.8-5	0.4-0.9
Gain [dB]	**70**	77	78	36	34
NF [dB]	**3**	2.6	3.1	5	4
NF @-4dBm blocker at 20MHz offset [dB]	**10/12**	>20	15	-	-
IB-IIP_3 [dBm]	**+6**	-7.5..0	-12.4	-3.5	+3.5
OB-IIP_3 @20MHz [dBm]	**+10**	-17..-4.6	-	-	-
IIP_2 [dBm]	**+70**	+53..+59	+45..+50	+45..+65	+51
$B_{1dB,CP}$ @20MHz [dBm]	**>-8**	-30	~-9	-	<-20
Power cons [mW]	**30-55*** **(64-100)**	66-143	55mA from battery	68-98*	60*
Area [mm^2]	**2**	2	2.44	6.96*	1*

* does not include synthesizer, IB-IIP_3 @LNA-1st, min gain - OB-IIP_3 @max gain.

Figure 3.6.6: State-of-the-art overview of SDR receivers.

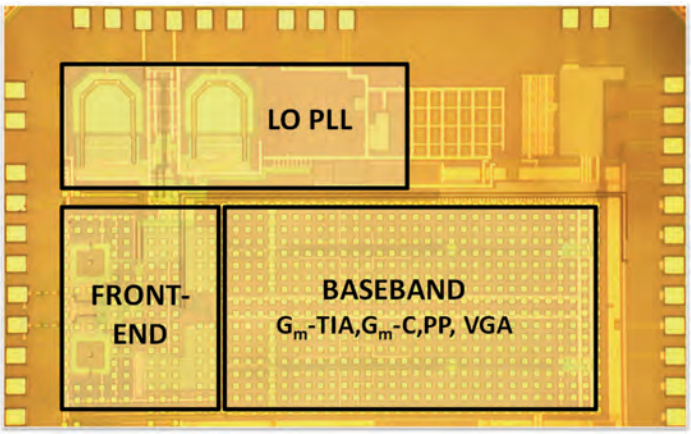

Figure 3.6.7: Chip micrograph.

978-1-61284-302-5/11/$26.00