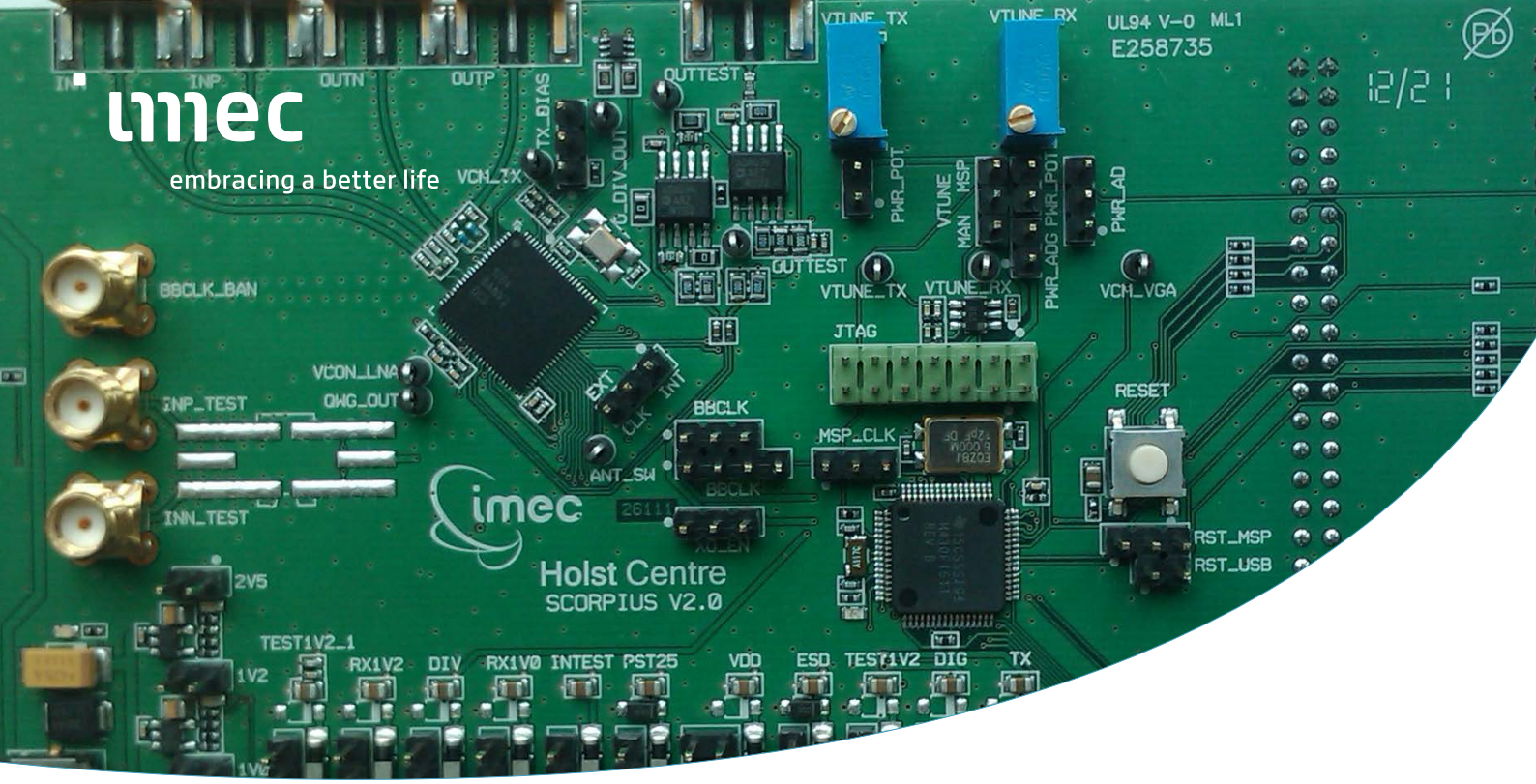


9BIT SAR ADC FOR ULTRALOW-POWER WIRELESS SENSOR NODES IN 40nm CMOS

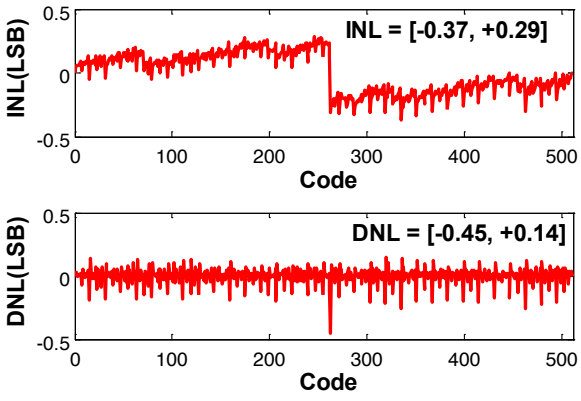
DESCRIPTION

This ADC has 9bit resolution and can support sample rates from DC to 12.5MS/s, this design can be used for a variety of applications such as sensor interfacing and receiver frontends (e.g., BLE, Zigbee, 802.11.ah).

BLOCK DIAGRAM

The differential input signal voltage is sampled on the capacitor arrays inside the DAC. The binary-scaled DAC uses unit capacitor as well as the monotonic switching scheme to save power, which are switched between GND and VDD. The small value of unit element minimizes the power consumption while providing sufficient kT/C noise performance for 9bit resolution. The asynchronous logic control resolves the bits of the output code based on self-synchronization. Thus, this architecture requires only a sample-rate clock instead of an over-sampled clock.

Static performance: INL/DNL



The measurement presented is done at 1V. The INL and DNL at are 0.37LSB and 0.45LSB at 1V.

KEY FEATURES

Low-power techniques

- Asynchronous dynamic logic
- Monotonic switching scheme

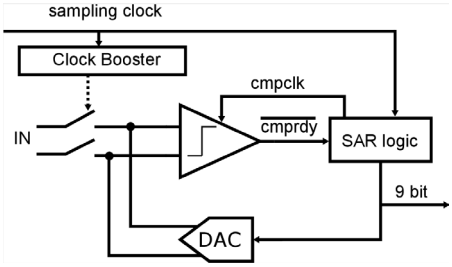
Excellent performance

- Power consumption: 30.4µW@1.0V supply
- FoM: 6.7fJ/conv.step@1.0V
- Max. INL/DNL <0.5LSB@1.0V
- Leakage: 23nW@1.0V
- Dynamic power consumption from 0 to 12.5 MS/s

No calibration

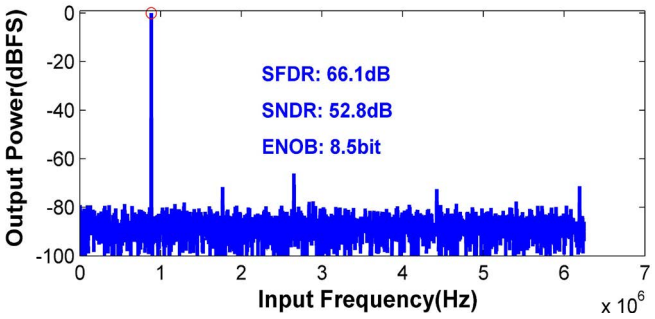
APPLICATIONS

- Wireless sensor nodes

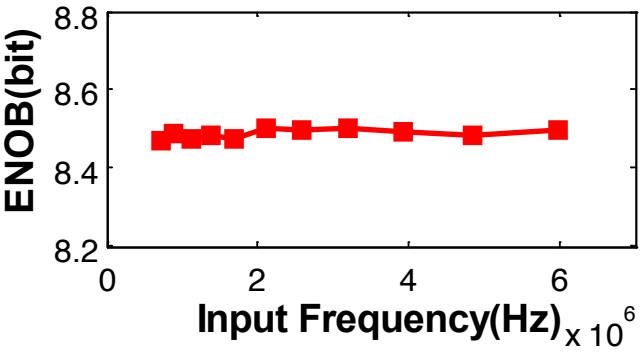


SPECTRUM AND DYNAMIC PERFORMANCE

The spectrum of the ADC is shown below. The achieved SFDR is 66.1dB, which is sufficient for a 9bit ADC. The achieved SNDR is 52.8dB, which is equivalent to 8.5bit ENOB.

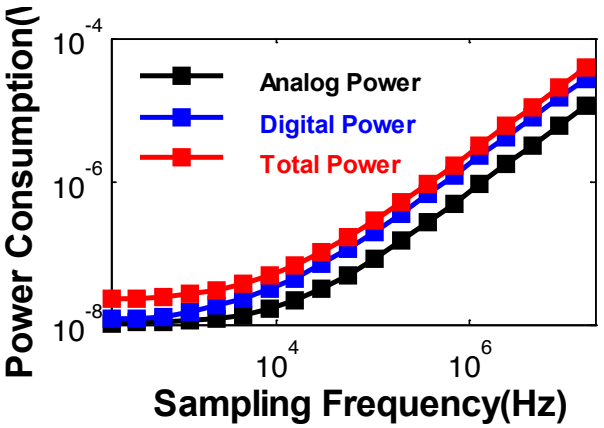


The ENOB versus signal frequency is shown. It reaches up to 8.5bits with an ERBW beyond Nyquist at 1.0V supply.



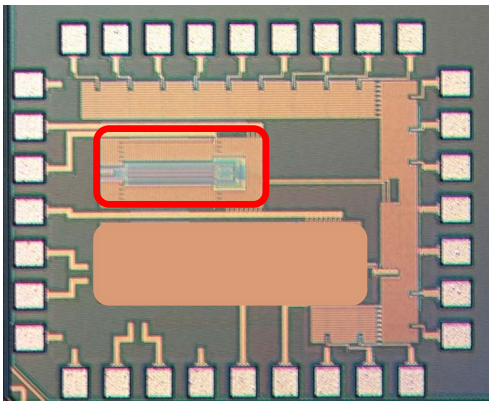
POWER CONSUMPTION

The power consumption of the ADC at 1.0V is shown below. The energy per conversion is 2.432pJ: 0.711pJ from the analog and 1.721pJ from the digital. The dynamic power consumption scales with the sampling rate down to 23nW.



MEASUREMENT RESULTS

Technology	40nm CMOS
Resolution	9bit
Chip area	134µm*312µm
Input capacitance	0.73PF
Max. INL/DNL (LSB)	0.45
Supply (V)	1.0
Common-mode level (V)	0.4
Sampling rate (MSps)	12.5
(pp) Signal range (V)	1.67
Power consumption (µW)	30.4
Leakage (nW)	23
ENOB (bit)	8.5
FoM (fJ/conv.step)	6.7



Note: there is an updated version of this chip, which is optimized for higher speed. It can operate up to 16MS/s, which can be used for BLE 5.0.

EVALUATION BOARDS

Imec provides evaluation boards (EB) on request to prospective customers and partners interested in licensing imec's radio designs and IP.

AMERICAS
raffaella.borzi@imec.be
T +1 408 386 8357

CHINA
timo.dong@imec-cn.cn
+86 13564515130

EUROPE & ISRAEL
michel.windal@imec.be
+32 478 96 67 29

JAPAN
isao.kawata@imec.be
T +81 90 9367 8463

TAIWAN & SE-ASIA
mavis.ho@imec.be
T +886 989 837 678

VIETNAM, BRAZIL, RUSSIA, MID EAST, INDIA
max.mirgoli@imec.be
T +1 415 480 4519